HEWLETT-PACKARD

COMPUTER MAINTENANCE COURSE

VOLUME XVI

STUDENT MANUAL

HP 3030 MAGNETIC TAPE SYSTEM

(HP STOCK NO. 5950-9204)

-NOTICE-

The information contained in this manual is for training purposes only. Consult the Hewlett-Packard documentation supplied with the computer for current information concerning the specific computer system furnished.

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SPECIFICATIONS AND PERFORMANCE CHARACTERISTICS

1-1. INTRODUCTION.

1-2. Hewlett-Packard D-3030G-H01 Tape Units are designed for use with the HP 12559A Interface and an HP 2116, 2115, or 2114 Digital Computer. This configuration is capable of reading and writing IBM standard computer 9-track format tapes at a tape speed of 75 inches per second with bit-packing density of 800 bits per inch. D-3030 Tape Units include electromechanical tape handling mechanisms, magnetic read/write/erase heads, operator controls and indicators, load-point and end-of-tape photosensing, file protect devices, and all necessary power supplies.

1-3. All assemblies are mounted within a sturdy cabinet. A full-length, hinged front cover door contains a counterbalanced sliding panel to provide convenient access to the transport for tape loading and threading. A single, front-access card rack, located behind three panels adjacent to the vacuum chambers, houses the data electronics circuit cards and the cards containing control and logic circuits associated with the operation of the tape transport. A rear door provides access to other assemblies within the cabinet.

1-4. D-3030 Single Tape Units are tape transports complete with data electronics. The units accept data inputs at logic levels suitable for writing and supply reproduced data which is detected, converted to appropriate logic levels, and clocked out from output registers. Pulse data operation is also available as a standard production operation.

1-5. SPECIFICATIONS.

1-6. Excluding the specifications for the data electronics and accessories, the specifications given in the following paragraphs apply to the D-3030G-H01.

1-7. DIMENSIONS.

1-8. External dimensions of the Tape Unit cabinet are 29-5/8 inches wide by 69 inches high by 25 inches deep. Tape Units may be installed in side-by-side contact and require no separation clearance for opening cabinet doors. A clearance of 28 inches is required in front of the Tape Unit to permit the cabinet door to be opened a full 90 degrees.

1-9. INPUT/OUTPUT CONNECTORS.

1-10. Primary power (J2), tape unit control (J1), data input (J4), and data output (J5) connectors are located at the lower rear of the cabinet on a reversible panel to allow connecting cables to be brought in through the rear of the cabinet or up thorugh the bottom of the cabinet. Mating connectors for J1 (36 pins), J4 (20 pins), and J5 (20 pins) are supplied on the interface cables.

1-11. CONTROL INPUT AND STATUS OUTPUT SIGNALS.

1-12. Control and status signals are carried by the 36-pin connector J1 to and from the control and logic section of the Card Rack.

1-13. TAPE MOTION CONTROL INPUT SIGNALS. Input circuits are transistor triggers strapped for positive negative levels and true or false logic at the time of manufacture. The triggers are always self-biased to the inactive state; that is, the driving circuit need only supply current (true logic) or absorb current (false logic) while holding a line in an active state. This arrangement results in fail-safe operation if the Tape Unit becomes disconnected from its associated equipment. Inputs requirements are summarized in table 1-1. The four tape motion control input signals and their operations are as follows:

a. FORWARD (negative true): the forward tape drive is maintained for as long as the command input level is maintained.

b. REVERSE (negative true): the reverse tape drive is maintained for as long as the command input level is maintained.

c. REWIND (negative true): a momentary (20 microseconds) input level initiates the Rewind cycle. Control logic selects a slow (75 ips) or fast (reel-to-reel) rewind speed, depending upon the amount of tape on the takeup reel. The tape is automatically repositioned to Load Point at the end of the Rewind cycle.

d. UNLOAD (negative true): a momentary (20 microseconds) input level initiates the Unload cycle. It has the same command and response characterisitcs as Rewind, with the additional response that the tape unit is switched to the LOCAL mode and accepts no further commands from the computer interface.

1-14. TAPE MOTION INTERLOCKS. To prevent damage to the tape and tape unit, several interlocks are incorporated in the tape unit. Simultaneous FORWARD and REVERSE inputs are automatically rejected; however, REWIND or UNLOAD inputs occurring while the unit is in forward or reverse drive are stored and executed when the drive input is removed. During REWIND, both the write and erase circuits are disabled.

1-15. STATUS OUTPUT SIGNALS. The status outputs from the tape unit consist of voltage levels (9 ± 1 volts and 0 ± 0.5 volts) from transistor line driver circuits. The circuits are strapped during manufacture to provide positive true output logic. With the output at "zero" level, the source impedance to ground is 100 ohms and the maximum

Table 1-1. Input Circuit Voltages

LOGIC	INPUT TERMINAL VOLTAGE		TERMINATION
	COMMAND PRESENT	COMMAND ABSENT	
(-) True	-3 to -15	-0.5. to +12	2.2 KΩ to gnd
(-) False	-0.5 to +12	-3 to -15	4.7 KΩ to -10V
(+) True	+3 to +15	+0.5 to -12	2.2 KΩ to gnd
(+) False	+0.5 to -12	+3 to +15	4.7 KΩ to +10V

allowable current is 10 milliamps. With the output at a positive or negative level, the source impedance to the 10-volt supply is 570 ohms and the maximum allowable current is 20 milliamps. The following signals are the status outputs to the external equipment.

a. READY ($\overline{\text{AUTO}}$): tape is threaded, vacuum is applied, and the tape unit is in the Automatic mode and ready to accept commands (control inputs).

b. REWIND ($\overline{\text{REWIND STATUS}}$): the tape unit is in the REWIND mode.

c. LOAD POINT ($\overline{\text{LOAD POINT STATUS}}$): the tape is positioned at the Load Point photoreflective marker and the tape unit is in READY status.

d. WRITE ENABLE ($\overline{\text{WRITE ENABLE}}$): the Write Data Electronics are enabled and the tape unit is in READY status.

e. END-OF-TAPE ($\overline{\text{EOT}}$): the EOT photoreflective marker is positioned under or has passed the photosense head since the last REWIND command was received and the tape unit is in READY status.

1-16. Although the density status indications are generated by the tape unit, they are not utilized by the interface.

1-17. In addition to the status outputs, an Address Switch contact closure, corresponding to the numeral showing on the Address indicator of the Control Panel, is normally sent to the external equipment. This feature is not utilized in the model H01.

1-18. DATA ELECTRONICS INPUT AND OUTPUT SIGNALS

1-19. The Data Electronics handles the Read and Write functions separately, with individual connectors to the data processing system for Write data inputs and Read data inputs and outputs. Input/output signals are transferred through connectors J4/P4 (Write) and J5/P5 (Read) to the data processing system.

1-20. The Write data inputs include nine channels of parallel logic level data signals, a WRITE PERMIT (WRITE ENABLE) input for external on-off control of the write heads, a WRITE RESET input for switching all head current to a common direction to write inter-record gaps, and a WRITE CLOCK input.

1-21. The Read Data inputs and outputs consist of a READ RESET input to set all output registers to the same state or to inhibit data output when desired, a READ CLOCK output, and nine channels of data output signals.

1-22. In addition, the Data Electronics receives inputs from tape unit control and logic circuits: a WRITE ENABLED input indicating that the supply reel is equipped with a Write Enable Ring, a REVERSE input to set certain skew compensation circuits when tape is read in the reverse direction. It should be noted at this point that the D3030G-H01 is capable of reading tapes recorded at any of the three densities, but due to the interface it may only record at 800 bpi.

1-23. MAGNETIC HEAD ASSEMBLIES.

1-24. The magnetic head assembly includes separate 9-track Write and Read head stacks, a full-track Erase head, a "head gate" to reduce write-to-read head coupling, and vacuum-cleaning tape guides. The write and read heads are 9-track IBM standard track widths and spacings. The center line of the first track is 0.029 inch from the top edge of the tape; succeeding tracks are centered at 0.055-inch increments, with a constant tolerance of ± 0.002 inch for each track center referenced to the top edge of the tape. The Write head track width is 0.048 inch and the Read head track width is 0.030 inch. Write-to-Read head gap spacing is 0.300 ±0.005 inch.

1-25. PERFORMANCE CHARACTERISITCS.

1-26. The performance characteristics of D-3030 tape units are presented in the paragraphs which follow. Included are brief discussions of tape motion characteristics, static and dynamic skew, types of data recording, power requirements, system reliability, and environmental conditions.

1-27. TAPE MOTION.

1-28. The following specifications apply to Tape Units operating at a tape speed of 75 ips from a regulated 60 cps (or 50 cps) AC line.

1-29. START CHARACTERISTICS. Within 5 milliseconds after the initiation of a Forward or Reverse command, tape speed will be within ± 5 percent of normal speed. Tape travel during the 5-millisecond start period will be within 0.185 ± 0.025 inch.

1-30. STOP CHARACTERISTICS. All tape motion will cease in less than 2 milliseconds after the removal of a Forward or Reverse command. No spurious signals will be generated after this time. Tape travel during the 2-millisecond stop period will be within 0.080 +0.010, -0.015 inch.

1-31. RUN CHARACTERISTICS. Average long-term speed deviation will be less than ± 1 percent. Speed deviation from average will be less than ± 1 percent when measured over tape lengths as short as 1.5 inches and less than ± 1.5 percent when measured over tape lengths as short as 0.135 inch.

1-32. ACTUATOR CHARACTERISTICS. The tape drive acuation system will accept any sequence of commands without causing damage to the Tape Unit or to the tape. A minimum of 5 milliseconds must be allowed between rapid sequential commands (FORWARD, STOP, REVERSE, STOP, etc.) if specified start and stop distances are to be maintained. More frequent commands may be programmed in sequences where the start or stop distances are not critical.

1-33. REWIND TIME. A full 2,400-foot reel of tape will be rewound within 3 minutes after the initiation of the Rewind operation.

1-34. SKEW.

1-35. Pulses previously written simultaneously on two or more tape tracks may not be reproduced simultaneously because of imperfections in the mechanical tape handling system. Such time displacement error, or skew, is specified as the worst-case time displacement of a reproduced pulse of a character as referenced to any other reproduced pulse of the same character.

1-36. Maximum dynamic skew is 3.6 microseconds, the time band within which a reproduced pulse from any track of a character will occur when referenced to a reproduced pulse of any other track of the same character.

1-37. Maximum static skew is 6.0 microseconds, the time displacement of the dynamic skew band center to the reference track pulse. The static skew specification applies when measured without compensation. Static skew, however, is eliminated by compensation circuits in both the Write and Read Data Electronics.

1-38. RECORDING METHOD.

1-39. D-3030 Tape Units employ NRZI recording, compatible with all IBM 727- and 729-series tape units at 800, 556, and 200 bit-per-inch recording densities. In the Write process, current flows through the heads continously and magnetizes the tape to saturation. A bit (logic "one") is recorded on the tape by reversing the direction of the head current. In the Read process, the points of flux reversal recorded on the tape induce current pulses in the Read head and are interpreted as "one" bits. The absence of a pulse during the bit period is interpreted as a "zero" bit.

1-40. WRITE DATA ELECTRONICS FUNCTIONS. The Write Data Electronics accepts nine-channel parallel data at its input in the form of logic levels, converts the data to the NRZI form, and drives the nine write heads to record the data on tape. A WRITE RESET input permits the external control equipment to switch all head current to the common direction for writing inter-record and other gaps on the tape. A Write Permit (WRITE ENABLE) input provides for external on-off control of head current. The File Protect system has overriding "off" control of the head current.

1-41. The Write Data Electronics includes delay circuits in each channel for skew compensation to ensure that the recorded bit alignment on the tapes is within the tolerances required for 556 or 800 bpi densities. Also included are circuits to drive the erase head, when writing is enabled and permitted, and circuits to compensate for any pulse asymmetry characteristics in the individual Write heads.

1-42. READ DATA ELECTRONICS FUNCTIONS. The Read Data Electronics amplifies the outputs of the nine read heads, detects the recorded "one" bits, and strobes the "one" bits constituting each character into an output register. The data output consists of nine logic levels at the output register and a clock pulse. A READ RESET input permits the external control equipment to set all the output registers of the Tape Unit to the same state and to inhibit tape unit data output when desired.

1-43. The Read Data Electronics includes circuits to change the read detection threshold, whenever data is being written, from a normal 20 percent of full pulse amplitude to 40 percent, in order to detect incipient data dropouts during a Read-After-Write mode of operation. Additional circuits detect the "one" bits at the time of their pulse peaks: this reduces the time displacement error caused by pulse amplitude variations. Also included are static skew compensation circuits for each channel, delay circuits for both forward and reverse directions of tape travel, and circuits to sense the direction of tape travel and switch the delays accordingly.

1-44. LATERAL PARITY GENERATION AND CHECKING. Lateral Parity generation and checking are functions of the interface circuitry. An "odd" number of "ones" is always maintained when writing data characters. This same condition is checked for during read operations.

1-45. INPUT POWER REQUIREMENTS.

1-46. Input power to the Tape Unit is 117 volts ac, single phase. A Tape Unit with Data Electronics requires 600 watts standby, 750 watts average operation, and 970 watts peak. The equipment will meet all specifications when operated on line voltages of 105 to 126 votls ac at line frequencies of 58 to 62 cps. Speed variation specifications apply only under conditions of precise power line frequency.

1-47. SYSTEM RELIABILITY.

1-48. System reliability includes data reliability, in terms of drop-outs or falsely injected signals caused by defects in tape or electronics, and equipment reliability, in terms of mean time to failure and preventive maintenance requirements. All figures pertaining to tape life are for recordings made at a density of 200 bpi on 1.5-mil, Mylar-base hard oxide tape of a recognized computer brand and quality.

1-49. WRITE ERRORS. Write errors, detected in a Read-After-Write mode with the Data Electronics threshold set at 40 percent, will not exceed 30 per reel of tape.

1-50. READ ERRORS, LONG PASSES, Reading tapes which have no Read-After-Write errors with the Data Electronics threshold set at 20 percent, there will be not more than one permanent error per 150 reels of tape. A permanent error is one that cannot be cleared after five rereads or by cleaning the read head surface.

1-51. READ ERRORS, SHORT PASSES. Reading a section of tape which does not have any initial errors detected in a Read-After-Write check and with the Data Electronics threshold set at 20 percent, there will be not more than one permanent error per 10,000 passes of a 10-foot length of tape.

operation [redacted]

SECTION II
OPERATION

2-1. GENERAL.

2-2. Since the Hewlett-Packard D-3030 Tape Unit is primarily intended to be operated automatically under the control of a data processing system, manual operations are limited mainly to changing tape reels and transferring control of the unit to the data processing system.

2-3. CONTROLS AND INDICATORS.

2-4. The controls and indicators and the parts of the tape transport associated with tape loading and threading are shown in Figure 2-1. The functions of the controls and indicators are given in Table 2-1.

2-5. It should be noted that during the AUTO mode of operation, when the tape unit is under the control of the computer system, the control panel pushbuttons (excluding the LOCAL pushbutton) are inoperative. The pushbuttons are enabled only when the LOCAL pushbutton has been actuated to switch control of the tape unit to the control panel.

2-6. PHOTOSENSE TABS.

2-7. Photosense tabs are supplied with a pressure-sensitive adhesive and should be attached to the non-oxide side of the tape as shown in Figure 2-2. The Load Point tab is to be placed along the edge of the tape nearest the operator. The End-of-Tape tab is to be placed along the edge of the tape nearest the transport.

2-8. APPLICATION OF POWER.

2-9. The D-3030 Tape Unit Control Panel does not have a power switch. Power to the Tape Unit is intended to be controlled as part of the system in which it is to function. It is assumed that power is applied to the tape unit at the same time that power is applied to the system.

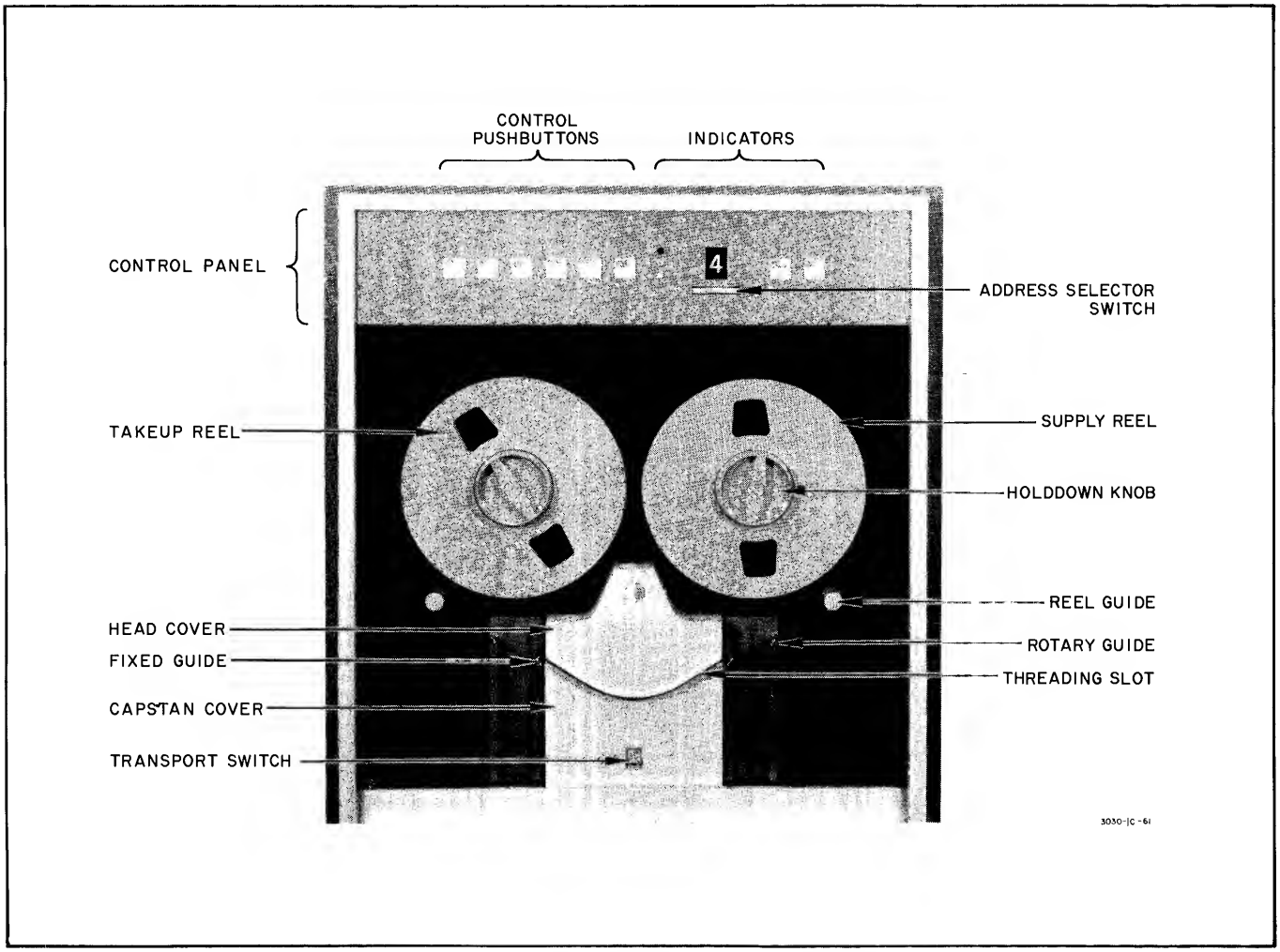


Figure 2-1. Operating Devices, Controls, and Indicators

Table 2-1. Functions of Controls and Indicators

CONTROL DEVICE OR INDICATOR	FUNCTION
LOCAL pushbutton	Switches control of tape unit to control panel; acts as emergency stop control. illuminated, tape unit is in LOCAL mode.
AUTO pushbutton	Switches control of tape unit to the computer system. When illuminated, tape unit is in automatic mode and all other pushbuttons (except LOCAL) are locked out.
LOAD POINT pushbutton	Indicates Load Point Search when tape unit is in LOCAL mode. When illuminated, tape is positioned at Load Point.
REWIND pushbutton	Switches tape unit to REWIND mode from LOCAL mode; causes transport to rewind tape to Load Point, initiates slow or normal rewind operation. When illuminated, tape unit is in REWIND mode.
REVERSE pushbutton	Drives tape in reverse direction as long as pushbutton is depressed.
CHANGE DENSITY pushbutton	When illuminated (LOCAL mode only), switches density operation of Data Electronics.
Density lamps (200,556,800)	Indicate density operating status of Read Data Electronics as set by CHANGE DENSITY switch.
Address numeral indicator	Indicates Tape Unit address (0 through 9) set by Address selector switch.
Address selector switch	Switches Tape Unit address (as shown in indicator above). Output to computer system from switch also indicates address. This feature is not utilized by the HP 12559A Interface.
WRITE ENABLED indicator	When illuminated, indicates that Write Enable Ring is installed on tape reel.
END OF TAPE indicator	When illuminated, indicates that End-of-Tape tab is under or has passed photosense head.
Transport Switch	START position (up): causes vacuum to be applied to chambers and tape to be loaded into chambers when tape is properly threaded. BRAKES position (down): releases reel motor brakes for tape threading; initiates DISABLED mode if actuated while Tape Unit is in LOCAL or AUTO mode. (Brakes circuit is bypassed during Rewind.) Center position is not connected to any circuit.
Cleaning Switch	Used only when cleaning pinchrollers and capstans. Up position: closes Forward actuator and starts capstan motor. Down position: closes Reverse actuator and starts capstan motor.

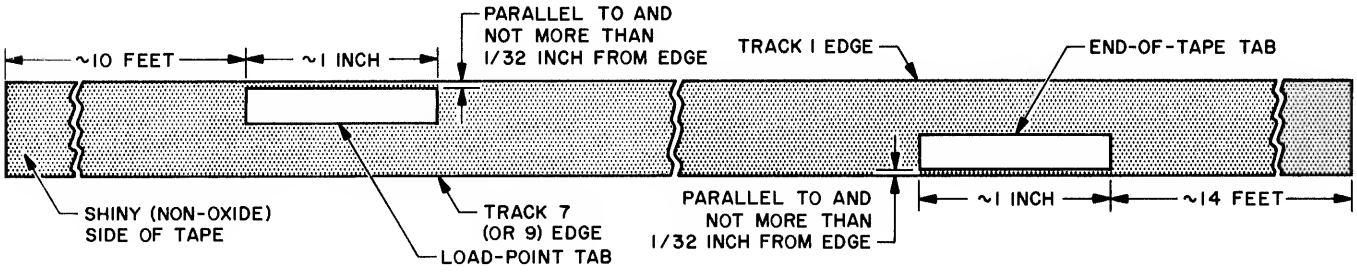


Figure 2-2. Location of Load-Point and End-of-Tape Photoreflective Tabs

2-10. MANUAL OPERATION.

2-11. Manual operations consist primarily of preparing the tape unit for automatic control: loading and threading the tape, advancing the tape to the Load Point, selecting the density and address required for the tape unit, and switching the tape unit to AUTO mode. If the tape unit has not received an UNLOAD command at the termination of the program, the tape must also be rewound prior to removing the tape reel from the tape unit.

2-12. REEL INSTALLATION AND TAPE THREADING.

2-13. If the tape reel to be installed is to be written upon (that is, the tape unit is to be operated in the WRITE mode), insert a plastic Write Enable Ring in the groove on the back of the tape reel (Figure 2-3). If the WRITE mode of operation is not to be used for that tape reel, check that the Write Enable Ring has been removed before installing the tape reel on the tape unit. Lower the slide panel in the front cover door for access to the tape transport.

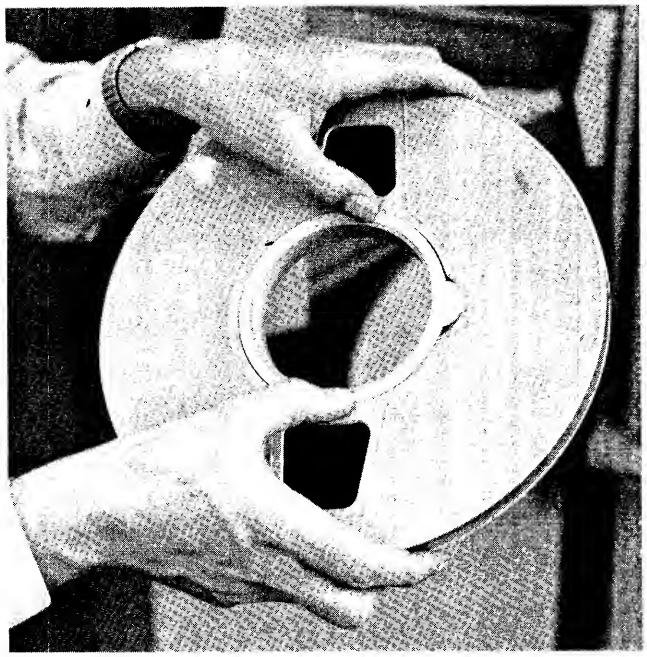


Figure 2-3. Write Enable Ring

a. Rotate the supply reel (right-hand reel) hold down knob fully counter-clockwise to relax the rubber grip ring.

b. Place the tape reel over the holddown knob and seat it firmly against the turntable by applying pressure only on the reel hub and not on the reel flanges. The Write Enable Ring groove around the hub should be nearest the tape unit, facing away from the operator.

c. While holding the reel firmly against the turntable, tighten the holddown knob (Figure 2-4) in a clockwise direction until it is snug or until the end-of-travel stop is reached.

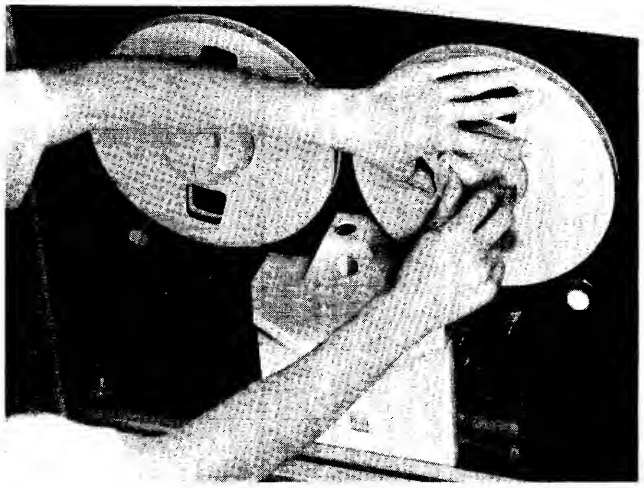


Figure 2-4. File Installation

d. Hold the Transport Switch in the BRAKES position (down) and pull about two feet of leader or tape from the supply reel (Figure 2-5). Release the Transport Switch, permitting it to return to the center position.

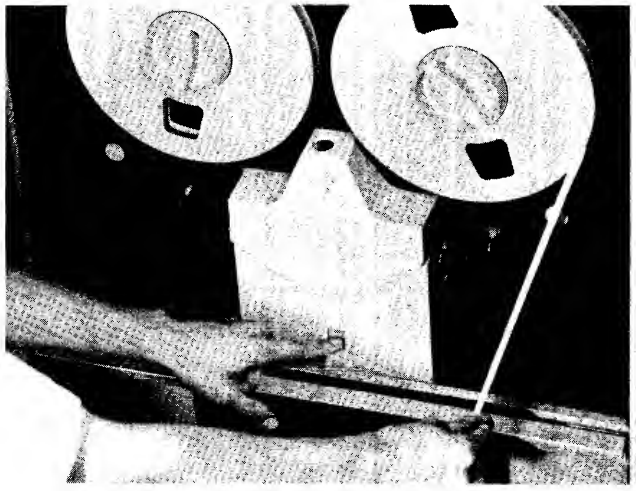


Figure 2-5. File Reel Leader

Note

The tape should unwind from the right-hand side of the tape reel. If this is not the case, check that the reel has been installed with the Write Enable Ring groove toward the tape unit. If the reel is installed correctly and tape unwinds from the left, the tape has been improperly wound and cannot be used on the tape unit. The oxide (non-shiny) side of the tape should be wound facing the hub of the reel. If the tape is wound oxide-side out, it cannot be used on the tape unit.

e. Grasp the tape with both hands and wrap it around the protruding lip of the head cover. Allow the slack loop of tape coming from the supply reel to hang outside of the reel guide.

f. Move the section of tape which is around the head cover inward and to the left, causing it to pass into the threading slot and engage with the driving components (Figure 2-6). Slide the tape back and forth a few times to ensure that it moves freely and lies straight over the chamber guides inside the glass (Figure 2-7).

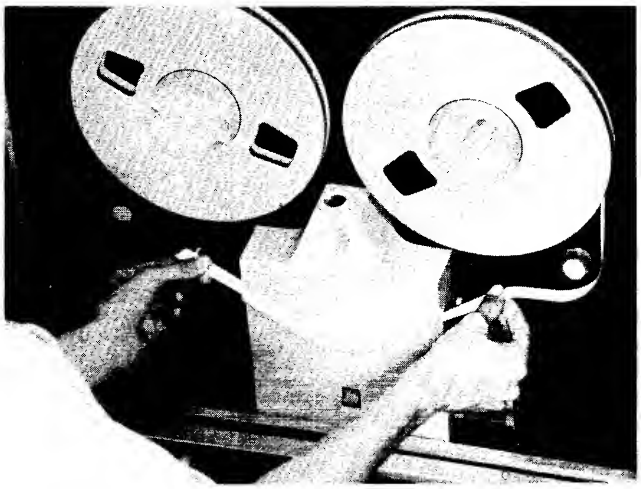


Figure 2-6. Threading Slot

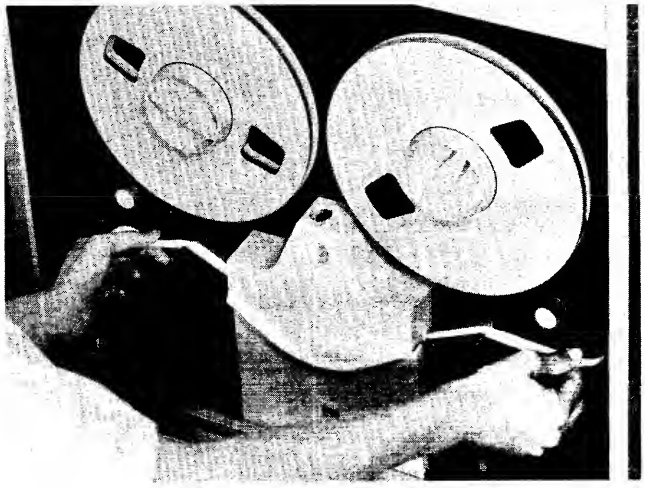


Figure 2-7. Tape Alignment

g. Pull the remainder of the slack tape through the left side of the head cover. Pass the tape under and around the outside of the takeup reel guide and drop the end of the tape between the takeup reel flanges onto the hub (Figure 2-8).

h. Hold the Transport Switch in the BRAKES position and wind about six turns of tape in a clockwise direction onto the takeup reel (Figure 2-9). When there is no slack in thre threaded tape path, release the Transport Switch. Check that the tape is aligned properly over the vacuum chamber entrances and that it passes around the underside of each reel guide.

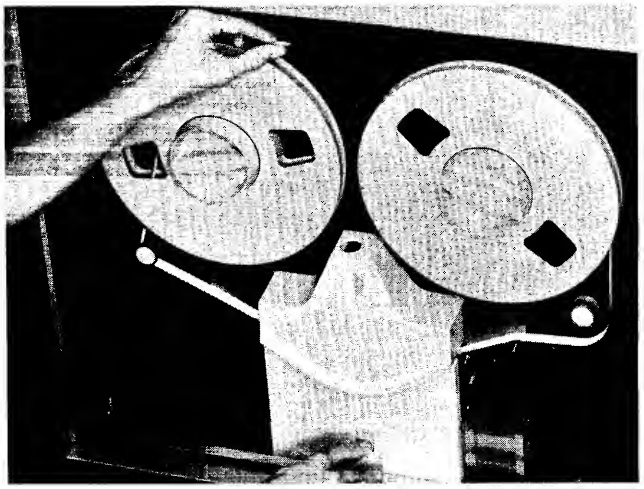


Figure 2-8. Takeup Reel Threading

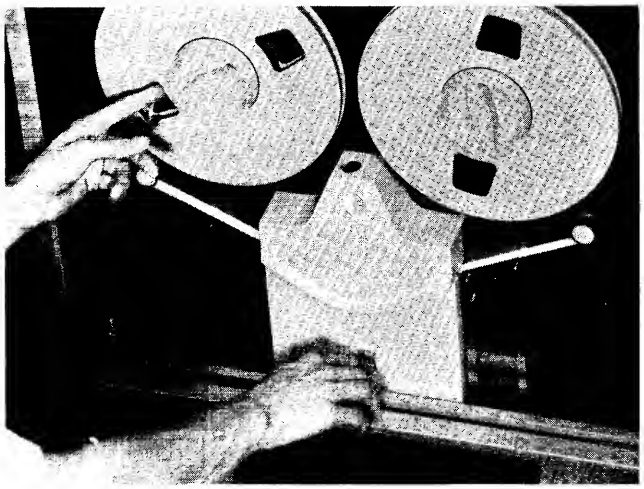


Figure 2-9. Takeup Reel Loading

i. Hold the Transport Switch in the START position (up). The capstans will start, vacuum will be applied, and the reel motors will feed tape into the chambers. When the reel motors stop, release the Transport Switch and close the front door slide panel. The tape unit is ready for operation.

2-14. ADVANCE TO LOAD POINT.

2-15. When the tape unit has been threaded and started, it will be in LOCAL mode of operation. Momentarily depress the LOAD POINT pushbutton. The tape will be driven forward until the Load Point tab is detected by the Photosense head, at which point the tape unit will stop. The LOAD POINT pushbutton is illuminated with the tape is at the Load Point.

2-16. DENSITY SELECTION.

2-17. The CHANGE DENSITY pushbutton is active (and illuminated) only when the tape unit is in the LOCAL mode. To set the tape unit for the bit-packing density of the tape reel, press the CHANGE DENSITY pushbutton until the lamp adjacent to the desired density (200, 556, or 800) is illuminated. It should be noted that if the tape is to be written on, the density must be set to 800 bpi.

2-18. TAPE UNIT ADDRESS SELECTION.

2-19. This feature is not utilized when the tape unit is connected through an HP 12559A Interface to an HP Computer.

2-20. LOCAL OR AUTOMATIC STATUS SELECTION.

2-21. To transfer control of the tape unit to the computer system, momentarily depress the AUTO pushbutton. The LOCAL pushbutton lamp will be extinguished and the AUTO pushbutton lamp illuminated. The tape unit is then in automatic mode and can be operated only from the computer system.

2-22. To return the tape unit to local control at any time momentarily depress the LOCAL pushbutton. The AUTO pushbutton lampwill be extinguished and the LOCAL pushbutton lamp illuminated. Any tape motion will stop, and control of the tape unit will be removed from the computer system.

2-23. REWINDING TAPE.

2-24. To rewind the tape from the takeup reel to the supply reel, the tape unit must be set to the LOCAL mode of operation. Momentarily depress the REWIND pushbutton to start the rewind operation. The pushbutton lamp will be illuminated and, depending upon the amount of tape stored on the takeup reel, the tape unit will perform either a fast (reel-to-reel) or a slow (normal Reverse speed) operation.

2-25. If the amount of tape to be rewound is small (as determined by the Pack Sense Photocell circuits), the tape unit drives the tape at normal Reverse speed until the Load Point tab is detected. At the Load Point, the Rewind operation stops. If the amount of tape to be rewound exceeds the predetermined amount, a reel-to-reel Rewind operation is automatically initiated.

2-26. First, the tape is removed from both vacuum chambers by a jogging motion of the reel motors. When both chambers are cleared, the tape is wound at high speed onto the supply reel. The fast rewind action continues until the amount of tape on the takeup reel decreases to the point where the Pack Sense circuits are energized. At this point, the Rewind circuits cause the tape loops to be restored in the vacuum chambers and a slow Rewind operation begins. The tape is driven at normal Reverse speed until the Load Point tab is detected. At the Load Point, the Rewind operation is terminated. Tape motion may be stopped at any time during a Rewind operation by depressing the LOCAL pushbutton.

2-27. REEL REMOVAL.

2-28. Before removing a tape reel from the tape unit, the tape must be rewound to the Load Point. The tape may then be stripped from the takeup reel manually or by using Reverse drive.

2-29. To strip the tape manually from the Load Point position, hold the Transport Switch in the BRAKES position. This places the tape unit in the DISABLED mode and releases the reel brakes. Wind the tape reel in a counterclockwise direction until all of the tape is wound onto the supply reel.

2-30. To strip the tape by using the Reverse drive after the Load Point is reached, depress and hold the REVERSE pushbutton to wind the tape off of the takeup reel. When the tape has been stripped from the reel, the end will snap into the left-hand chamber and the tape unit will switch to the DISABLED mode. When the transport has stopped, hold the Transport Switch in the BRAKES position and rotate the tape reel in a counterclockwise direction to wind the remaining tape onto the supply reel.

2-31. Turn the holddown knob counterclockwise to release the reel and remove the reel from the tape unit by grasping only the outer flange of the reel.

2-32. AUTOMATIC OPERATION.

2-33. In AUTO mode of operation, the tape unit is completely controlled by the computer system. The LOAD POINT, REWIND, REVERSE, and CHANGE DENSITY pushbuttons on the Control Panel are locked out so that an operator cannot inadvertently interfere with the remotely-controlled operation of the tape unit.

2-34. The computer system may also command the tape unit to perform a REWIND or UNLOAD operation. A Rewind command causes the tape to be rewound to the Load Point, and the Tape Unit remains in the AUTO mode to accept subsequent commands. An UNLOAD command (REWIND and STANDBY), however, not only causes the tape to be rewound to the Load Point, but also switches the tape unit to the LOCAL mode, removing it from automatic control.

2-35. ABNORMAL CONDITIONS.

2-36. Certain abnormal conditions may occur during operation to cause the tape unit to be placed in the DISABLED mode. It may also occasionally be necessary to manually stop the operation of the tape unit. Such conditions and the procedures for returning the tape unit to normal operation are described in the paragraphs which follow.

2-37. LONG OR SHORT LOOP.

2-38. Any condition which causes an abnormally long or short loop in either vacuum chamber will stop the tape unit and place it in the DISABLED mode. If the abnormal loop condition is corrected by the tape unit within one-half second, the tape unit will restart automatically. If the condition is not corrected, the tape unit will remain in the DISABLED mode and, after clearing the tape, must be restarted manually by moving the Transport Switch to the START position.

CAUTION

Before restarting a tape unit which has switched to the DISABLED mode, hold the Transport Switch in the BRAKES position and wind any slack tape onto one of the reels. The tape unit can then be restarted safely by operating the Transport Switch to the START position.

2-39. When the tape unit is disabled, it also switches from AUTO to LOCAL status, as indicated by the illumination of the LOCAL pushbutton. To return control to the computer system, the AUTO pushbutton must be depressed.

2-40. POWER FAILURE.

2-41. A power failure of more than one-half second duration will cause the tape unit to switch to the DISABLED mode. (Momentary failures may not stop the operation of the tape unit.) Before restarting the tape unit, refer to the CAUTION in paragraph 3-38. The AUTO pushbutton must also be depressed to return control to the computer system.

2-42. EMERGENCY STOP.

2-43. Any tape motion, whether initiated when the tape unit is in the LOCAL or AUTO mode of operation, can be stopped by momentarily depressing the LOCAL pushbutton. To restart the tape unit, move the Transport Switch to the START position. The AUTO pushbutton must also be depressed to return control to the computer system.

2-44. MANUAL DISABLE.

2-45. If, for any reason, it is desired to place the tape unit in the DISABLED mode while tape is still threaded on the unit, first stop any tape motion (remove the drive command, depress the LOCAL pushbutton, etc.) and make sure that the unit is transferred to the LOCAL mode. When tape motion has stopped, hold the Transport Switch in the BRAKES position until vacuum is removed from the chambers. Before restarting, check that the tape is properly threaded and positioned over the guides at the chamber entrances. To restart the tape unit, move the Transport Switch to the START position. The AUTO pushbutton must also be depressed to return control of the tape unit to the computer system.

detailed description

SECTION III
DETAILED DESCRIPTION

3-1. GENERAL.

3-2. The D-3030 Tape Unit (Figure 3-1) is a self-contained digital magnetic tape unit, with the cabinet forming the principal mounting structure for support of the major sub-assemblies. The sub-assemblies are the Control Panel, Tape Transport, Card Rack, Vacuum Plate, Vacuum Motor Deck, Power Supply, and Cover Door. These and other components are assembled and interconnected within the cabinet to form a single functional unit.

3-3. TAPE TRANSPORT.

3-4. The main components involved in transporting the tape are shown in Figures 3-2 and 3-3. The tape reels and reel motors are located side by side on the upper portion of the Tape Drive Plate. The drive section includes the chamber entrances, capstans, pinch roller actuators, and read/write heads and is located on the center of the Tape Drive Plate directly below the reels. The capstan drive motor is mounted on the back of the Tape Drive Plate. The vacuum chambers extend from the Tape Drive Plate to the Vacuum Plate, which supports the cambers where they connect to the vacuum manifold. The area behind the unsupported chamber sections is occupied by the Card Rack, in which the transport and data electronics circuit cards are housed. On the rear of the Vacuum Plate are the vacuum valve assembly and a number of vacuum switches. Directly behind the Vacuum Plate and mounted on the cabinet base is the Vacuum Motor Deck, which supports the vacuum motor and its capacitor. The Power Supply chassis is mounted on the cabinet base behind the Vacuum Motor Deck.

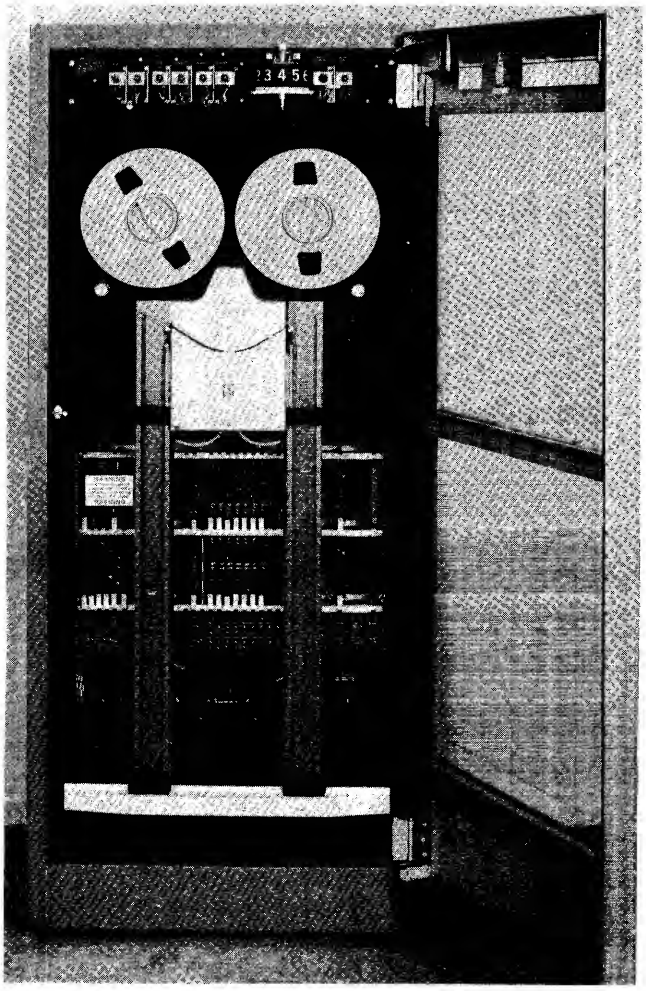


Figure 3-1. D-3030 Tape Unit

3-5. In this section, a typical D-3030 Tape Unit is described, first in terms of the hardware and then in terms of circuit operations. For descriptive purposes, the tape unit consists of functional sub-units such as the tape transport, data electronics, vacuum system, etc.; however, these sub-units do not exist as physically separable packages. For example, no single assembly forms a tape transport or the data electronics. The transport and data circuit card share the same card rack, and power supplies for both are contained on the same chassis.

3-6. TAPE PATH.

3-7. The tape path is shown in Figure 3-4. The tape emerges from the right-hand side of the supply reel and passes under a reel guide which positions the tape so that is will lie flat across the chamber entrance when threaded and be pulled in the chamber when vacuum is applied. The tape passes from the reel guide to a rotary guide at the chamber entrance and into the chamber to form a storage loop between the reel and drive components. At the exit side of the chamber, the tape moves over a buffer pocket post, a vacuum buffer pocket, which reduces starting transients, and a fixed guide. The tape then passes between the reverse capstan and pinchroller, above the Photosense head, and under the head assembly. The head assembly has a precision edge-loading guide at the entrance and exit and contains the Erase, Write, and Read head stacks, respectively. The tape path from the head assembly to the takeup reel is the reverse of the path from the supply reel to the head assembly, omitting the Photosense head.

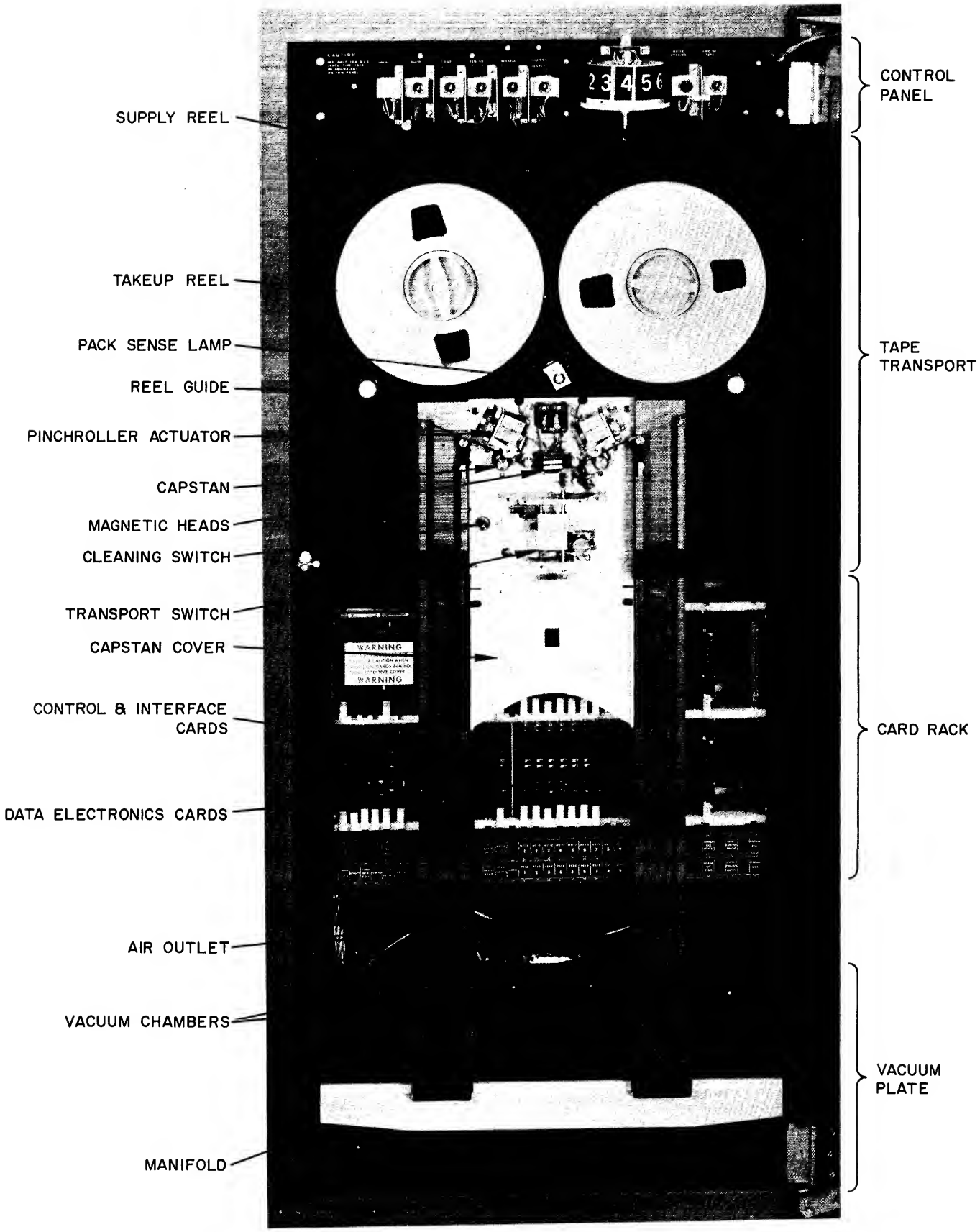


Figure 3-2. Front View of D-3030 Tape Unit

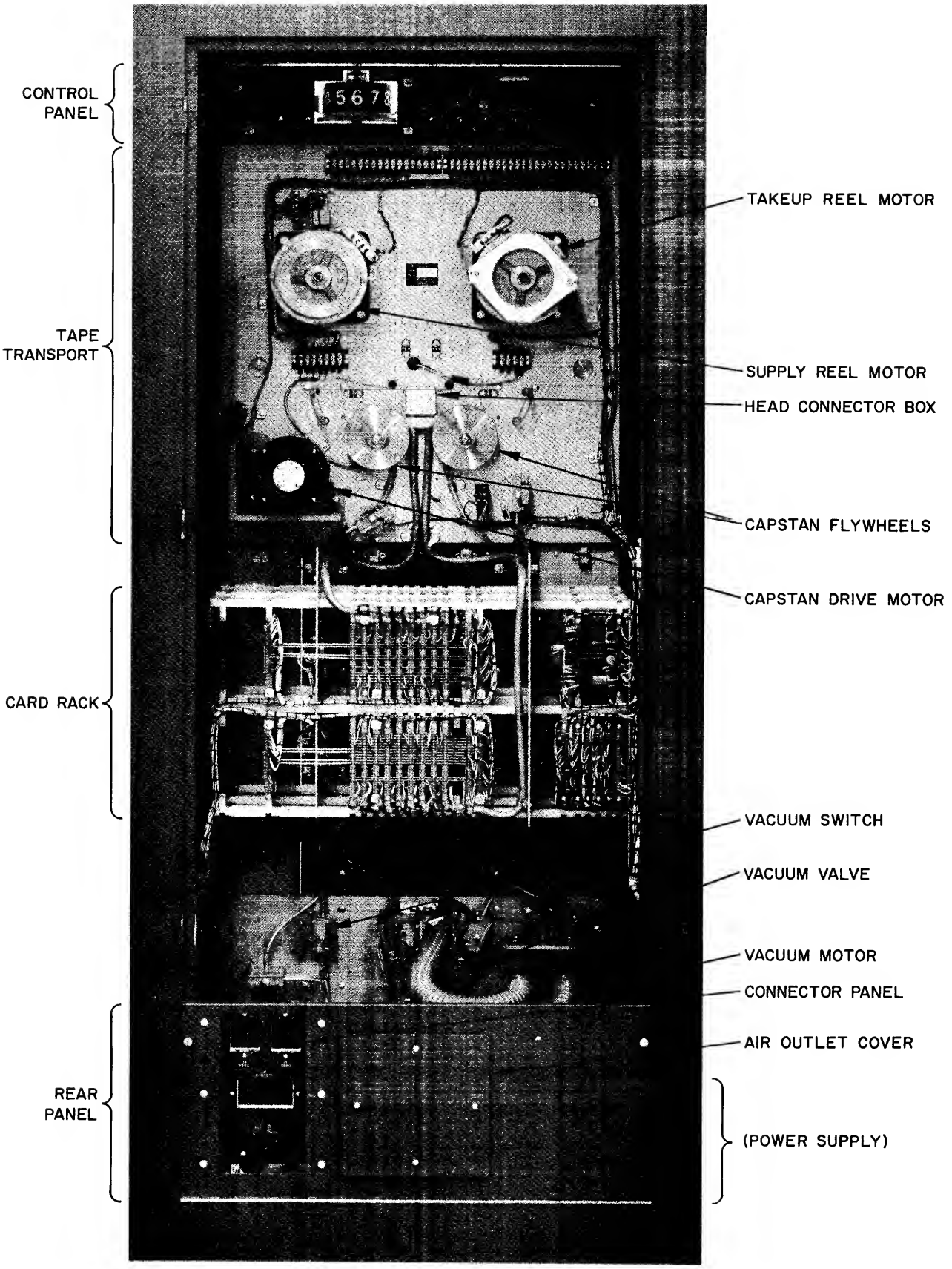


Figure 3-3. Rear View of D-3030 Tape Unit

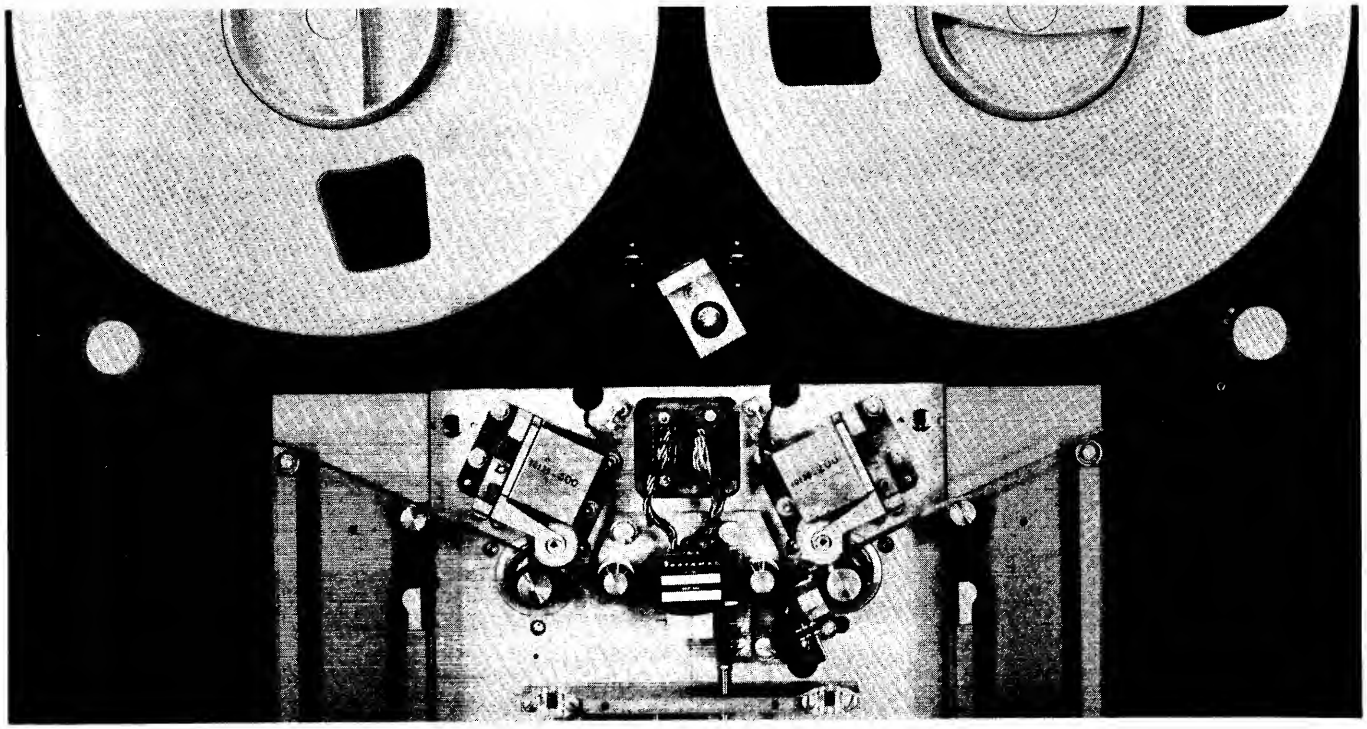


Figure 3-4. Tape Path

3-8. REEL MOTOR ASSEMBLIES.

3-9. Supply and takeup reel motor assemblies (Figure 3-5) are identical, except for the addition of a drag brake on the takeup reel motor to provide hold-back tension during high-speed rewinding. The reel motor is a series-wound DC motor with two sets of field windings. Power is applied to the motor through one or the other of the field windings, depending upon the direction of rotation desired. A reel turntable is mounted directly on the front of the motor shaft and is equipped with a quick-disconnect reel holddown device. The reel holddown grips the smooth inside surface of a tape reel by radially expanding a rubber grip ring. As the knob is advanced axially, the ring is compressed between the knob and the turntable.

3-10. A disc brake assembly mounted on the rear end of the motor contains a coil housing, brake disc, and brake rotor. The brake rotor is securely attached to the rear extension of the motor shaft and is faced with a disc of neoprene-impregnated cork brake lining. The hard, chrome-plated steel brake disc is forced axially against the rotor brake lining by a compression spring working against the motor end bell. The brake disc, retained by two nylon pins, is free to move axially, but prevented from rotating. Braking torque is developed by friction between the stationary disc and the brake rotor. A small air gap exists between the stationary disc and the brake rotor. A small air gap exists between the stationary disc and coil housing. Wehn current flowing through the coil sets up a magnetic field sufficient to overcome the force of the brake spring, the disc is attracted to the coil housing, leaving the rotor free to turn. Whenever power is applied to either of the motor filed windings, it is simultaneously applied to the brake coil. The time constant of the brake coil and circuit is such that from 30 to 50 milliseconds are required for current to build up to release the brake. The time required for the magnetic field to decay and engage the brake is of about the same value. Since the stall torque of the motor is about one-half the brake torque, the motor shaft cannot begin to rotate until the brake is released.

3-11. The drag brake, on the takeup motor assembly only, utilizes a spring-loaded plate and attached flat plastic ring to apply pressure to the back of the brake rotor. Drag brake friction is adjusted by two moveable brackets and is normally set to provide a drag of 5 to 6 inch-ounces measured at the takeup reel hub.

3-12. VACUUM SYSTEM.

3-13. The vacuum system controls the lengths of buffer tape loops stored in the chambers between the reels and drive section. This is accomplished by means of vacuum in the chambers and a number of vacuum sensing switches, as shown in Figure 3-6. The difference in pressure above and below the tape in the chambers maintains the loops in a taut condition and provides a constant source of hold-back tension on tape passing over the heads. The vacuum switches sense the positions of the tape within the chambers and control the reel motors and other electrical functions of the tape unit. A valve assembly controls the

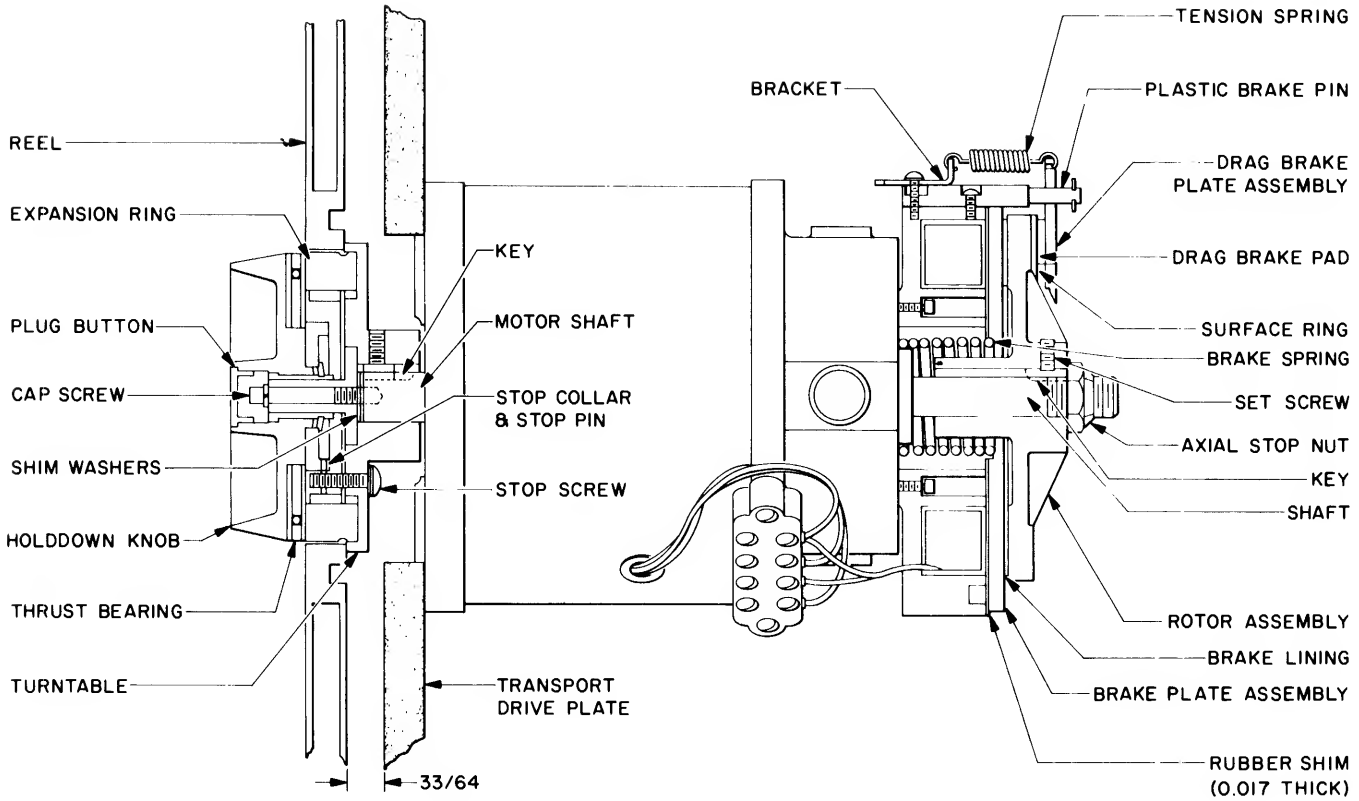


Figure 3-5. Takeup Reel Motor Assembly

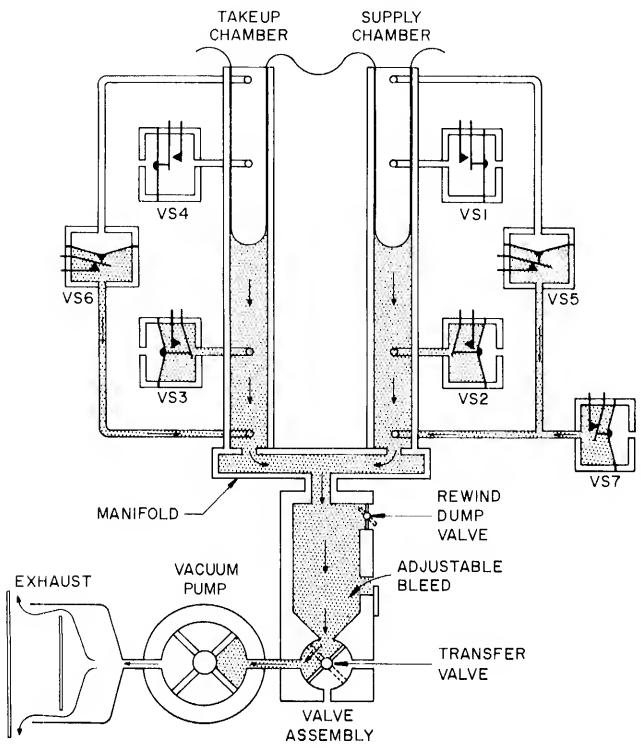


Figure 3-6. Vacuum System Diagram

chamber vacuum under different modes of operation. The vacuum pump provides a vacuum for the system and is also the source of air used to cool certain electrical components.

3-14. VACUUM MOTOR DECK AND AIR OUTLET. The vacuum motor is a self-contained motor and pump assembly mounted on the Vacuum Motor Deck (Figure 3-7). The motor is a split-phase, two-pole, capacitor-operated induction type, which eliminates the need for frequent servicing and does not contribute contaminants from brush and commutator wear. Two hose connectors near the top of the assembly enable connection to the input and output of the vacuum pump. The motor base is attached to the deck by four resilient rubber mounts. Two similar mounts and a stabilizing bracket extending from the Vacuum Plate support the top of the motor. The vacuum Motor Deck also contains the motor capacitor and a terminal block, TB13, through which power is supplied to the motor. The vacuum motor operates when power is applied to the tape unit and the transport power switch, S1, on the Power Supply chassis is turned on. The motor circuit is protected by fuse F3 on the Power Supply.

3-15. Pump motor cooling is provided by the air flow through the vacuum system. Under normal running conditions, the pump maintains a vacuum of about 20 inches of water at a flow rate of about 25 cfm. The exhaust air is channeled through a flexible hose to the Air Outlet assembly mounted on the rear panel of the Cabinet. A cross-sectional view of the Air Outlet is shown in Figure 3-8.

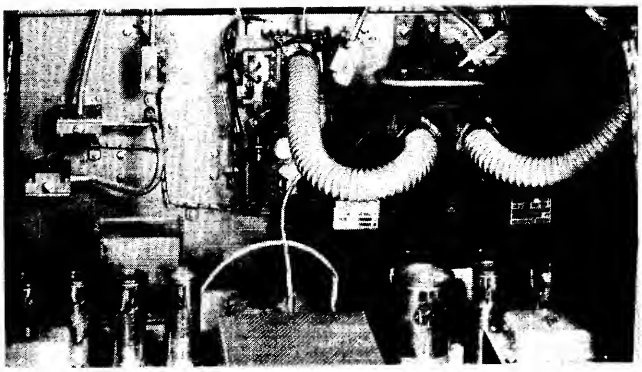


Figure 3-7. Vacuum Motor Deck

Exhaust air passes through the Air Outlet, cooling the reel brake resistors (R19, 20, 21, and 22) mounted on a heat sink within the assembly body, and exits through a narrow slot between the assembly body and cover plate. Electrical connection to the resistors is made through a four-terminal plug and socket (P6 and J6) located on the base of the Air Outlet body.

3-16. VALVE ASSEMBLY. The valve assembly (Figure 3-9) performs three functions: transfers vacuum to and from the vacuum chambers, provides an adjustable bleed valve to set the running vacuum level, and reduces the vacuum applied to the chambers during Rewind. The assembly is mounted near the center of the Vacuum Plate and is connected to the vacuum pump inlet by a flexible hose.

3-17. The transfer valve connects the vacuum source to the chambers when the tape unit is in operation. In the DISABLED mode, the valve removes all vacuum from the chambers by opening a vent port to prevent tape from being drawn into the chambers during threading. In the vent position, the valve also connects the vacuum source to an inlet port to allow cooling air to continue to flow through the vacuum motor. The transfer valve is operated by a solenoid and return spring; when energized, the solenoid overcomes the return spring force anc connects the vacuum source to the chambers.

3-18. The vacuum-adjusting bleed valve is located on the outside of the valve assembly body in a position which permits air to be bled into the system between the chambers and transfer valve. During tape unit operation, the vacuum developed is inversely proportional to air flow and leakage into the system. The total air flow comprises leakage around the tape loops in the chambers, air entering the tape cleaning guides on the head assembly, and air entering through the bleed valve. The bleed valve is adjusted manually to set the desired operating vacuum level.

3-19. When a high-speed Rewind is performed, the vacuum level must be reduced by about one-half so that tape can be removed from the chambers and wound directly from reel to reel. This is accomplished by opening the solenoid-acutated rewind dump valve to cause more air to enter the system. The amount of opening is controlled by the stroke length of the solenoid, and the position of the solenoid relative to the valve operating lever is adjustable.

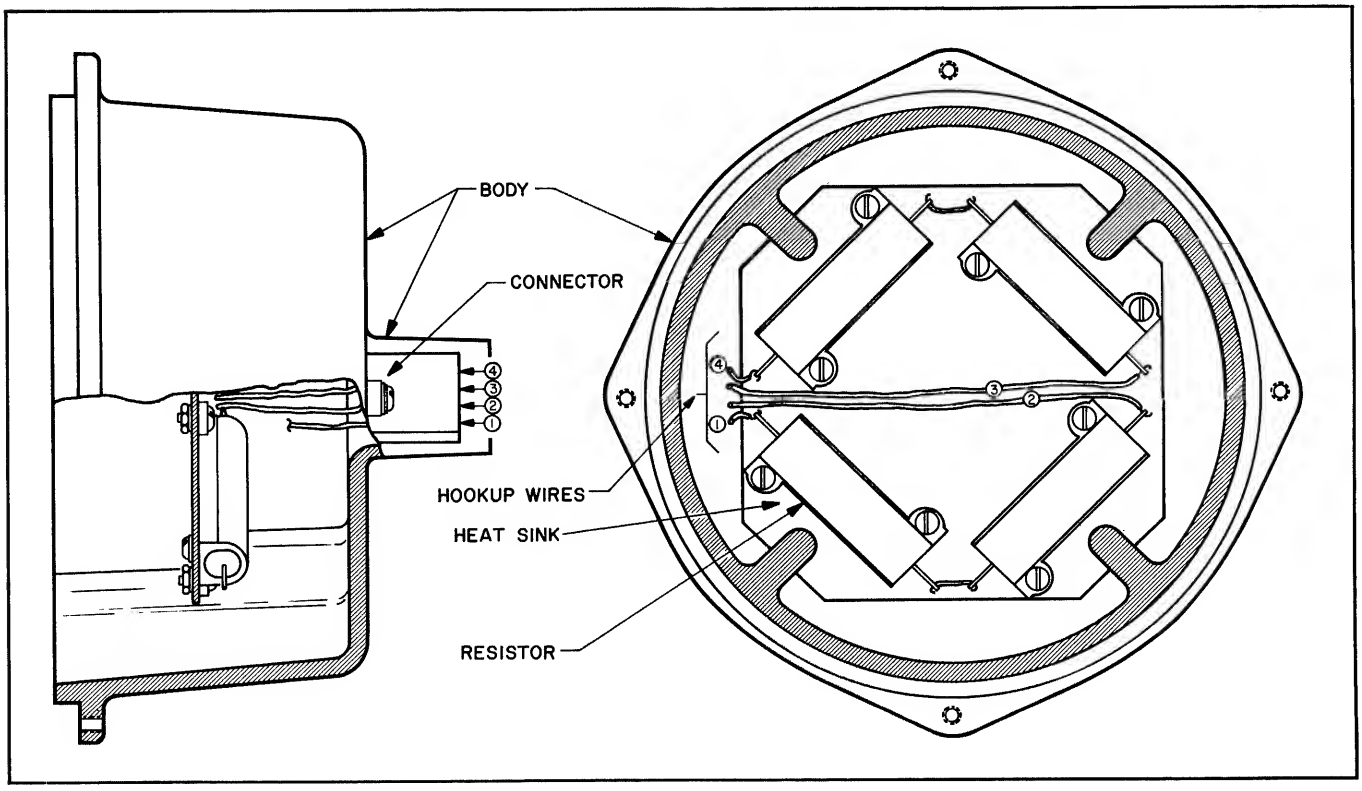


Figure 3-8. Cross-section of Air Outlet

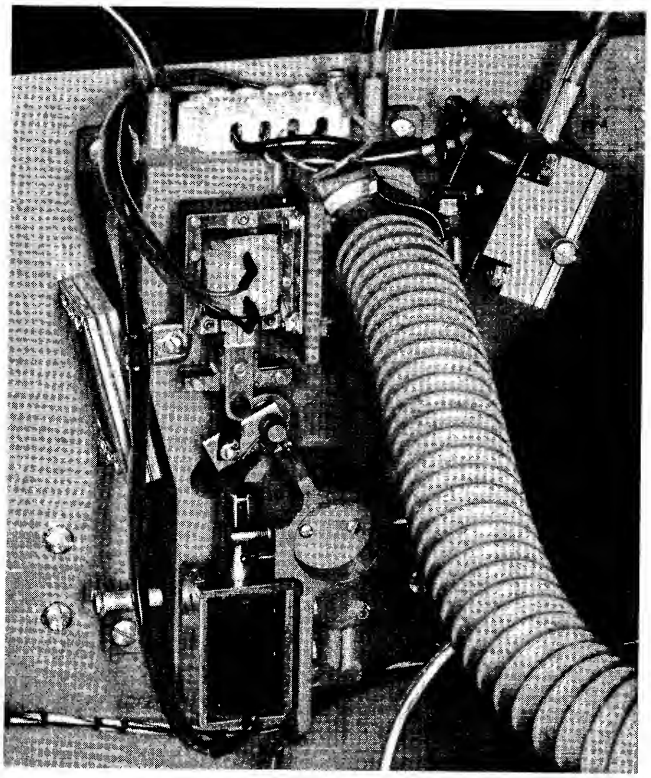


Figure 3-9. Vacuum Valve Assembly

3-20. VACUUM CHAMBERS AND MANIFOLD. The vacuum chambers are constructed from a precision aluminum alloy extrusion, the surfaces of which are hard-anodized to prevent wear from the cutting action of the tape edges. The chamber sidewalls are covered with a low-friction glass bead material to minimize tape sticking due to static electricity. Each chamber is covered with a hinged glass door, and vacuum is applied to the closed ends of the chambers through a manifold coupled to the vacuum source.

3-21. Tape enters a chamber over a non-magnetic, metal rotary guide, forms a storage loop in the chamber, and exits over a fixed non-magnetic metal guide. Below the fixed guide, a vacuum buffer pocket located in the chamber wall provides a small unsupported tape loop to reduce tape overshoot when the pinchroller is closed, which results in more rapid damping of the tape starting transient.

3-22. The position of a tape loop within a chamber is sensed by vacuum switches, as shown in Figure 3-6. The two inntermost sensing holes in a chamber each connect to a separate vacuum switch (VS4 and VS3, VS1 and VS2) to operate the reel and servo motors. The two outermost sensing holes connect to opposite sides of a single vacuum switch (VS6 or VS5) and actuate a normally closed alarm circuit whenever a tape loop is too long or too short. As long as a pressure differential exists across an alarm switch, the circuit is closed. Loss of the pressure differential (vacuum on both sides of the switch diaphragm or atmospheric pressure on both sides) causes the circuit to open.

3-23. VACUUM SWITCHES. Vacuum switches are used to detect the position of a tape loop within a vacuum chamber. The switches connect to vacuum sensing holes in the chambers with flexible plastic tubing. Pressure less than atmospheric pressure causes movement of a diaphragm which closes an electrical contract and applies a signal to the reel motors. A cross-sectional view of a normally open vacuum switch is shown in Figure 3-10. The switch consists of a body, diaphragm assembly, moveable contact, fixed contact, spacer, mounting bracket, vacuum nipple, and output terminals.

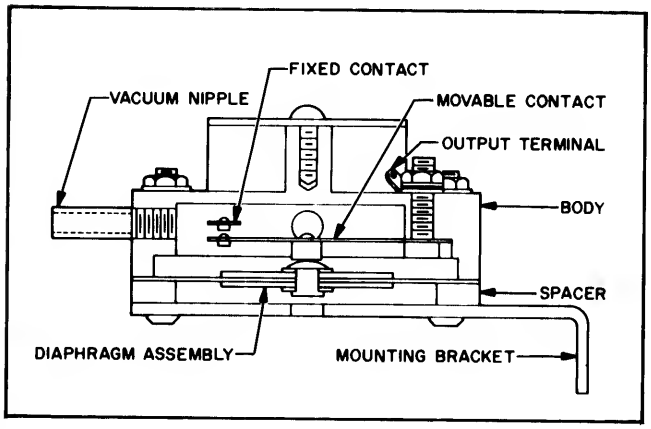


Figure 3-10. Cross-section of Vacuum Switch

3-24. CAPSTAN MOTOR AND CAPSTANS.

3-25. Two counter-rotating capstan assemblies (Figure 3-11) mounted on the Tape Drive Plate are driven by a single capstan motor through a pulley, flywheel, and belt arrangement. The capstans rotate at 1910 rpm to provide a tape velocity of 75 ips. The capstan motor assembly consists of a 3600-rpm synchronous motor on a cast aluminum mounting bracket. A crowned motor pulley is attached to the motor shaft, and the bracket has a surface for mounting the motor capacitor and a terminal board. A capstan assembly contains a bearing housing, capstan shaft, two sealed bearings, and a flywheel pulley. The bearings are double-sealed to prevent damage from oxide and other contaminants.

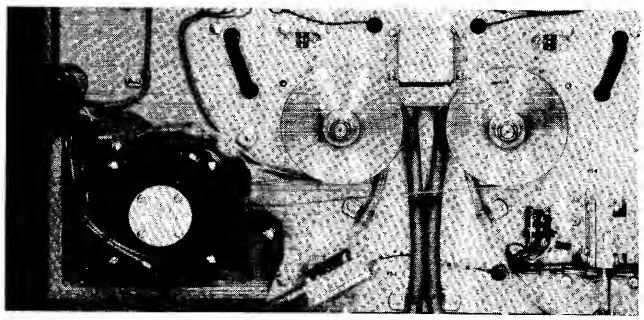


Figure 3-11. Capstans and Drive Motor

3-26. ACTUATORS.

3-27. Two actuator assemblies (Figure 3-12) are mounted on the front of the Tape Drive Plate. Each actuator and associated capstan produces one direction of tape movement as a result of the tape being forced against the rotating surface of a capstan by an actuator pinchroller.

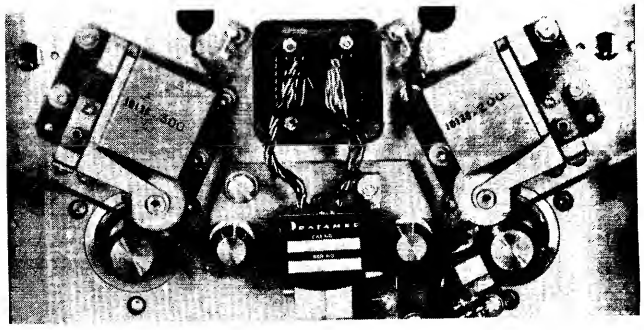


Figure 3-12. Actuator Assemblies

3-28. An actuator consists of a mounting base, solenoid, soilenoid housing, spring, spring mounting block, yoke, stop post, and pinchroller assembly. As shown in Figure 3-13, the yoke is free to pivot against the restoring force of a cantilevered spring. Yoke rotation is produced when the solenoid is energized and attracts the flat portion of the yoke.

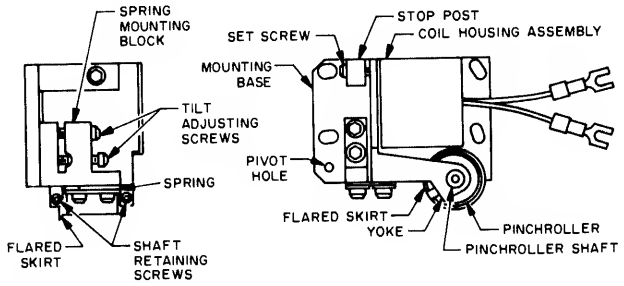


Figure 3-13. Actuator Parts Identification

3-29. The pinchroller assembly contains a rubber-covered aluminum roller shell, two miniature flange bearings, and a fixed mounting shaft. The inner race of each bearing rotates about the fixed shaft to enable the pinchroller to rotate while in contact with the capstan. A flexible, flared skirt on one end of the pinchroller maintains contact with the capstan when the actuator is open to keep the pinchroller rotating at all times. This provides more stable tape starting conditions since the pinchroller does not have to be accellerated when the actuator closes.

3-30. The de-energized position of the yoke is adjusted by a screw in the stop post. The spring mounting block is slotted and is adjusted by two screws to vary the tilt of the yoke to establish a parallel gap between the pinchroller and capstan. The entire actuator assembly pivots about a pin in the main frame which passes through a hole in one corner of the actuator mounting base. A bracket and adjusting screw mounted to the main frame permit adjustment of the actuator position so that the pinchroller contacts the capstan properly when the actuator closure is set correctly.

3-31. WRITE ENABLE ASSEMBLY.

3-32. The Write Enable assembly (Figure 3-14) consists of a base plate, spring-loaded actuator, solenoid switch, and terminal strip and is mounted on the rear of the Tape Drive Plate directly above the supply reel motor. The actuator protrudes through a hole in the Tape Drive Plate to detect the presence or absence of a Write Enable Ring on the file reel.

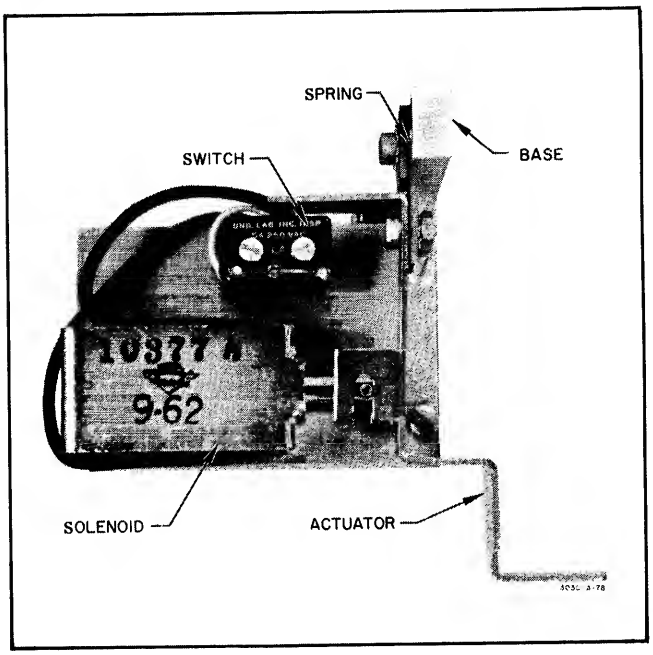


Figure 3-14. Write Enable Assembly

3-33. When a reel with a Write Enable Ring is placed on the tape unit, the actuator is depressed and closes the switch (Figure 3-15). After the tape has been threaded and the transport started, a relay energizes the solenoid, which retracts the actuator. The switch closure also activates logic circuits which enable the Write Data Electronics and provide Write Enabled status indications. The solenoid remains energized until power is removed from the circuit by placing the tape unit in the DISABLED mode.

3-34. HEAD ASSEMBLY.

3-35. The Write head stack, Read head stack, full-width Erase head, two tape guide/cleaners, head gate, and base plate comprise the head assembly (Figure 3-16). The components are mounted on the base plate, which attaches to the Tape Drive Plate between the actuators. Leads from the head windings are terminated in a pair of connectors which mate with the connectors associated with the Data Electronics.

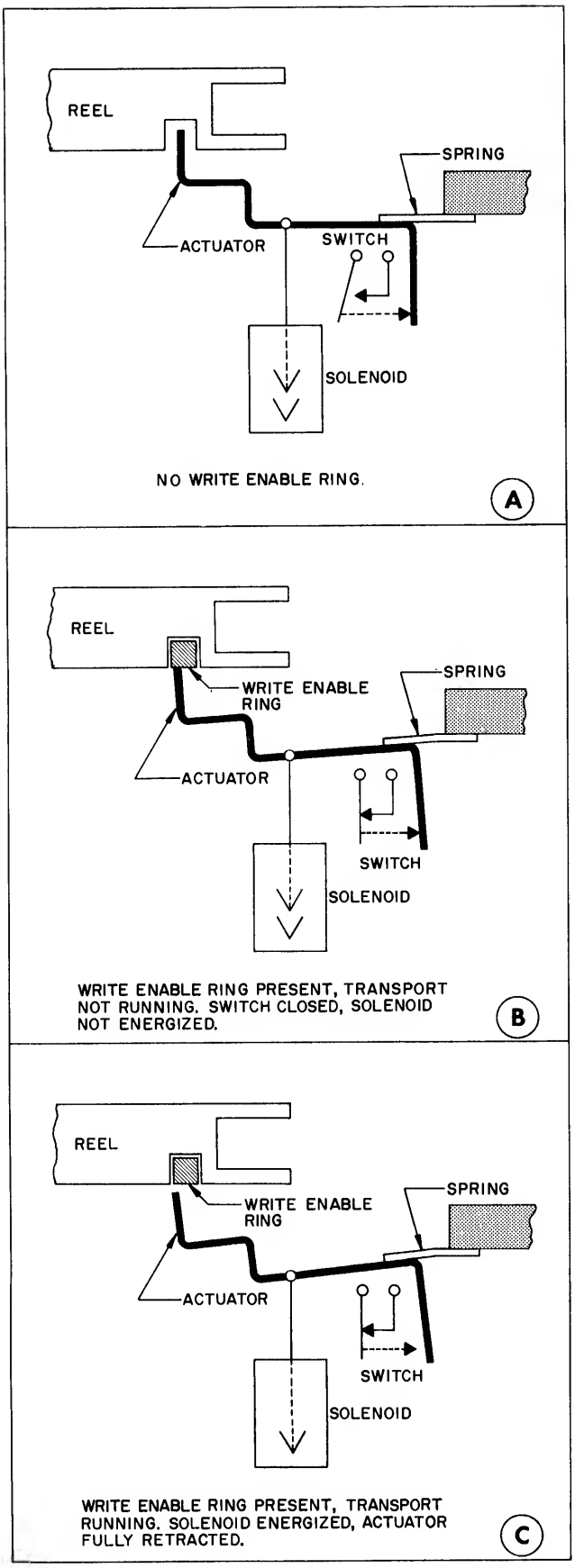


Figure 3-15. Write Enable Operation

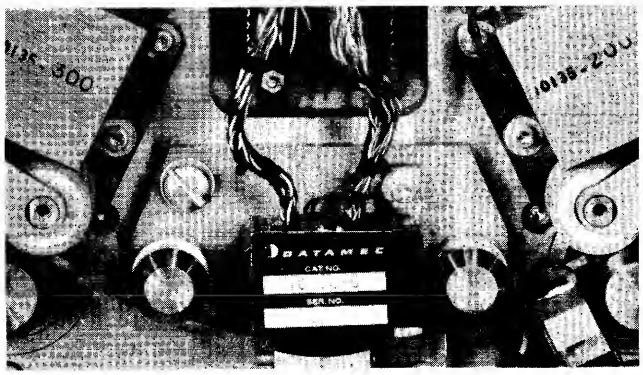


Figure 3-16. Head Assembly

3-36. In the Write head stack, each track consists of a magnetic circuit with a center-tapped winding and with a gap located adjacent to the tape. Current from one end of the winding to the center tap creates a magnetic field in the circuit. Fringing of the magnetic flux at the gap causes the flux to penetrate the tape and magnetize the iron oxide coating. When the current is switched from one end of the winding to the other, flux of opposite polarity is generated and causes a polarity reversal in the tape magnetization. Each point of magnetization reversal is considered a "one" in the coding scheme used in IBM-compatible magnetic tapes.

3-37. The Read head stack is similar to the Write head stack, although the individual read tracks are narrower, the windings have more turns of wire, and the gap in the magnetic circuit is smaller. As magnetized tape passes under a Read head, flux from any point of change in tape magnetization will thread through the magnetic structure and induce voltage in the winding.

3-38. The two head stacks are arranged so that tape passes under the Write gaps, then under the Read gaps, with a 0.300-inch spacing between the gaps. Since it is possible to read what has been written on the tape almost concurrently with the writing, the tape may be checked for accuracy during the writing process.

3-39. A tape/guide cleaner is located on each side of the head. The undersurface of the cap on each guide is lined with a hard ceramic washer which is precisely located to guide the tape as it passes under the head. The tape edge is held against this reference surface by a spring-loaded ceramic washer located on the inner side of the guide post opposite the cap. The guide post is hollow and slotted and connects to the vacuum system with plastic tubing. The slot is arranged so that, as tape passes under the guide, air sweeps over the face of the tape and into the slot. This action cleans away any loose particles of oxide or dust from the tape surface.

3-40. A hinged head gate attached to the front of the base plate serves to reduce write/read crosstalk. It is coupled to the Transport Switch slide rod and opens when the switch is moved to the BRAKES position. The head gate remains open until the switch is moved to the START position, closing the gate.

3-41. PHOTOSENSE HEAD ASSEMBLY.

3-42. The Photosense head detects the presence of reflective tabs placed on the Mylar side of the tape to indicate the beginning and end of a tape. It is located between the reverse capstan and head assembly, 1-3/4 inches from the Write head.

3-43. The relationship of the Photosense head to the tape and a tab is shown in Figure 3-17. A single lamp is located along the centerline of the tape, and directly above and below the light source are the photosensing elements. The photocells have built-in lenses and are positioned at an angle such that light from the lamp will be reflected from the associated tab into the lens. A mask over the lamp prevents unnecessary radient energy from striking the tape, reducing the heating effects of the lamp.

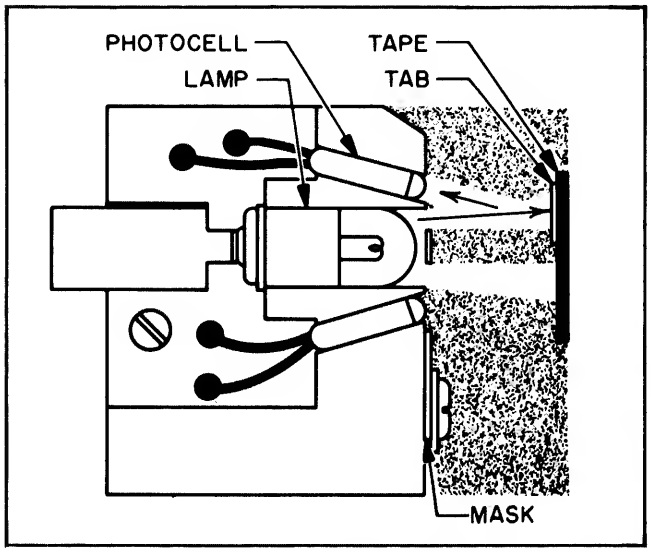


Figure 3-17. Photosense Head Assembly Operation

3-44. The photocell leads are brought out to a terminal board at the rear of the head. The lamp is held in place by a removable leaf spring which also serves as the center contact. Contact with the lamp base is made through the body of the head assembly. A cable connecting the lamp and photocells to the Photosense amplifier circuit card is permanently attached to the head.

3-45. PACK SENSING ASSEMBLY.

3-46. A lamp and lens assembly located above the head connector produces a beam of light which is used to sense the quantity of tape on the takeup reel. The beam is focused through the takeup reel to a photocell located on the bottom of the Control Panel.

3-47. As shown in Figure 3-18, the light beam is directed between the takeup reel flanges slightly to the right of the reel hub. When a tape pack of about 1/8-inch thickness has accumulated on the reel, the beam path is interrupted, activating the logic circuits which determine the rewind speed.

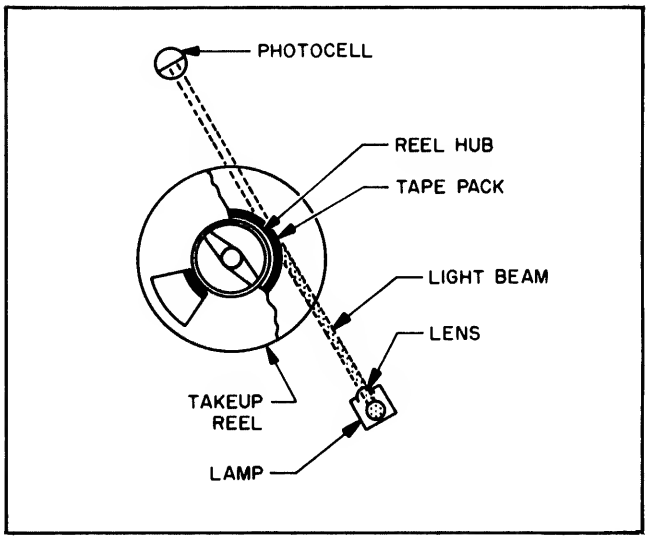


Figure 3-18. Pack Sense Assembly Operation

3-48. TRANSPORT AND CLEANING SWITCHES.

3-49. The Transport Switch (Figure 3-19) is a sliding switch handle located below the head assembly on the Tape Drive Plate and is accessible through a square opening in the capstan cover. The switch handle is mounted on two parallel rods which contain centering springs for the handle. Operation of the handle actuates microswitches which start the tape transport and release the reel brakes for tape threading. Through a linkage, it also opens and closes the head gate.

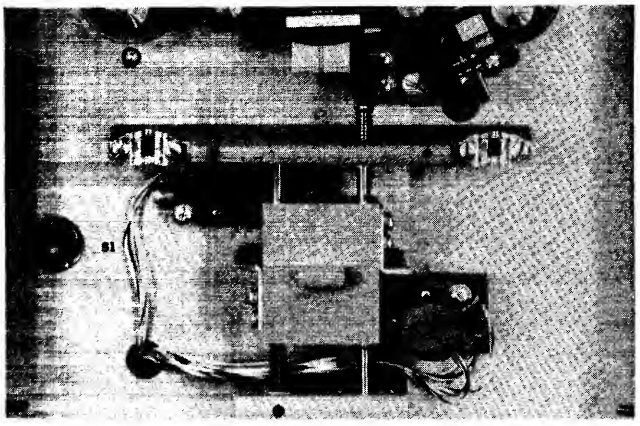


Figure 3-19. Transport and Cleaning Switches

3-50. To the left of the Transport Switch is the Cleaning Switch, a three-position, center-off toggle switch used to facilitate cleaning the capstans and pinchrollers. When the tape unit is in the DISABLED mode, operation of the Cleaning Switch starts the capstan motor and closes either of the two actuators.

3-51. COVERS AND REEL GUIDES.

3-52. Two cast covers protect components in the tape drive area and aid in tape threading. The head cover has a raised lip to provide a guide surface for threading the tape between the capstans and pinchrollers. It is held in place on the cabinet by four spring clips and can be completely removed for cleaning and servicing the tape drive section.

3-53. The capstan cover is hinged at the bottom and retained at the top by two strong clips. It can be opened, after the head cover has been removed, by pulling outward from the top of the cover. To open the glass vacuum chamber covers, it is necessary to open the capstan cover first.

3-54. A rotating reel guide is located below each tape reel outside of the corresponding chamber entrance. Threading tape under these guides causes the tape to lie flat across the chamber entrances so that it will be drawn into the chamber when vacuum is applied. A reel guide assembly (Figure 3-20) consists of a roller and shaft rotating on two ball bearings. The bearings are contained in a bearing housing which is retained by a collar and set screw. The collar is permanently mounted to the Tape Drive Plate. To adjust the distance of the reel guide from the Tape Drive Plate, the set screw is loosened and the bearing housing moved inward or outward.

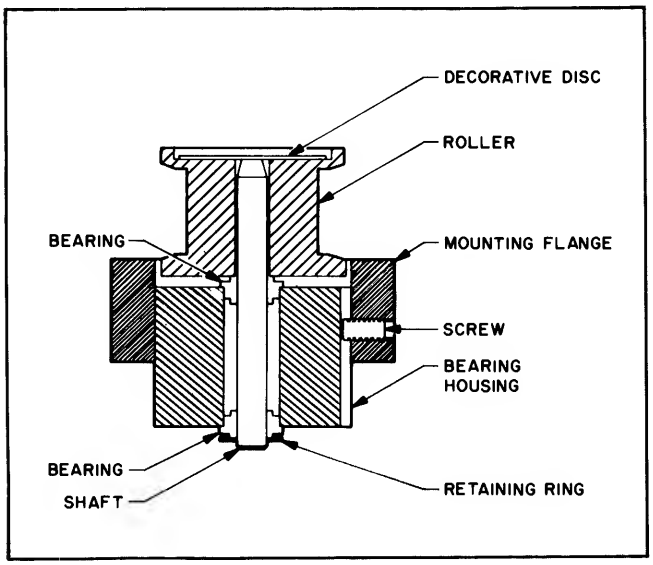


Figure 3-20. Cross-section of Reel Guide Assembly

3-55. CONTROL PANEL.

3-56. Switches and indicators associated with manual control of the tape unit are mounted in the Control Panel assembly shown in Figures 3-21 and 3-22. The principal structure of the assembly is a formed sheet-metal panel mounted on the cabinet frame above the Tape Drive Plate. Brackets which support the various switches and lamps are attached to the front panel. The pushbuttons, however, mounted on a panel which forms part of the Cover Door assembly (Figure 3-23).

357. The lamp sockets are threaded to accept colored plastic lenses. The tape unit is supplied with the red lens on the WRITE ENABLED lamp and an amber lens on the LOCAL lamp. A slot in the mounting bracket for each switch permits adjustment for proper travel when the pushbutton is depressed. The WRITE ENABLED and END OF TAPE indicator panels are held in place by a metal bushing when the Cover Door is closed.

3-58. A translucent plastic drum attached to the index mechanism of a rotary switch forms the Address indicator. At the bottom of the drum is a knurled wheel which protrudes through a slot in the Cover Door and provides the means for changing the address number of the tape unit. The address numbers are formed by a transparent mask wrapped around the outside of the drum. The drum is attached to the knurled wheel by three set screws. The position of the visible numeral relative to the switch position can be adjusted by loosening a set screw and rotating the drum. Vertical alignment of the Address indicator with respect to the panel opening is adjusted by loosening the set screw securing the knurled wheel to the switch shaft and sliding the wheel up or down. The address indicator lamp has a socket mounted on a spring clip; the socket is easily removed from the top of the assembly for changing lamps.

3-59. A flexible cable extends from one corner of the Control Panel to the three Density indicator lamps on the Cover Door panel. The cable is equipped with sockets which connect to pins on the back of the lamp assemblies. The indicators are integral lamp-jewel assemblies which attach to the panel with spring clips and must be replaced as a unit.

3-60. The Change Density stepping switch and several resistors and diodes used in certain lamp circuits are mounted on the back of the Control Panel. Near the bottom left-hand edge of the panel is the pack sensing photocell, which is exposed to the associated light source by a hole in the panel extending outward from the Control Panel. Connections to the Control Panel are made through a wiring harness which connects to barrier terminal strips located along the top of the Tape Drive Plate.

3-61. CARD RACK.

3-62. All circuit cards are housed in a single Card Rack which is located behind the vacuum chambers directly below the Tape Drive Plate. Figure 3-24 shows the Card Rack as viewed from the front, with the snap-out access panels removed from the tape unit. Figure 3-25 shows the connectors and wiring at the rear of the Card Rack.

3-63. The Card Rack is composed of a number of spacers and guides supported by rods. Each guide has an integral foot which serves as a mounting for a card connector. The entire assembly is held together by a pair of end plates and two bulkheads. This consturction sections the rack into three horizontal compartments, each with

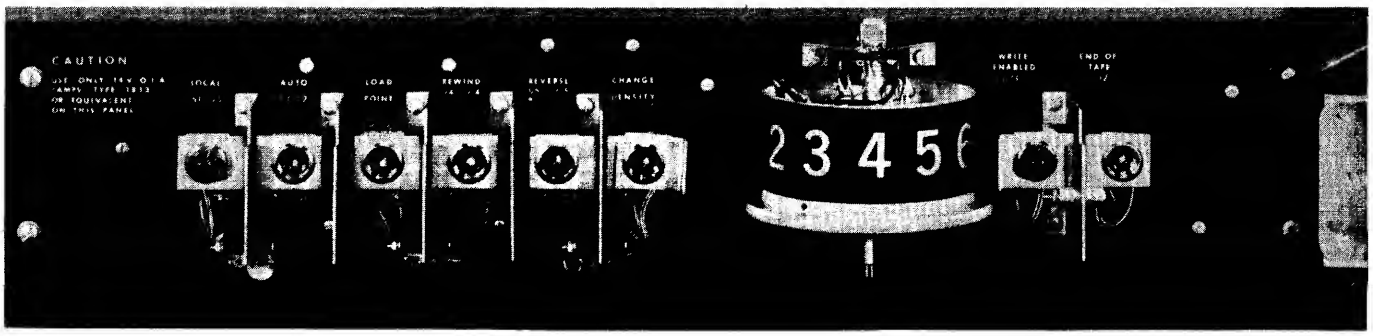


Figure 3-21. Front View of Control Panel Assembly

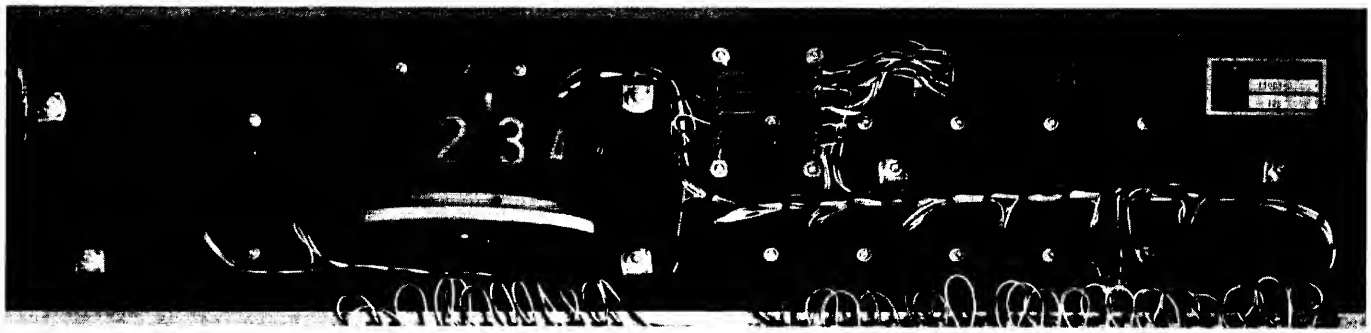


Figure 3-22. Rear View of Control Panel Assembly

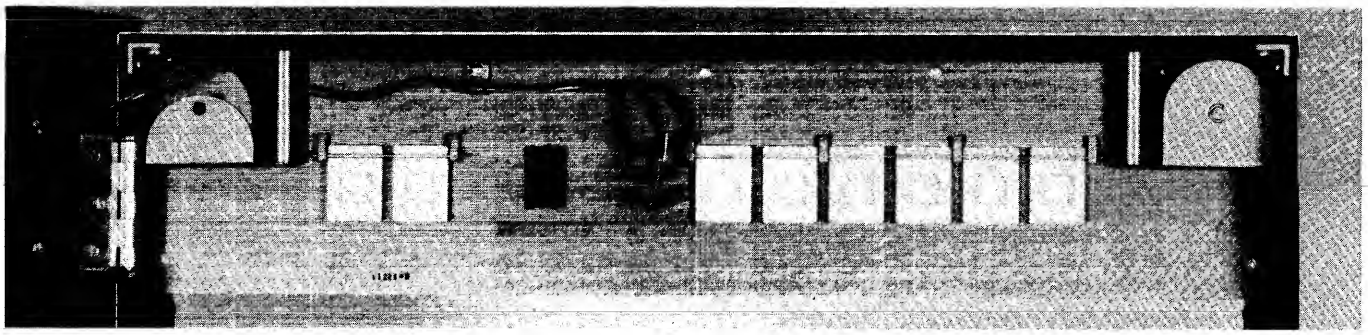


Figure 3-23. Top Rear View of Cover Door Assembly

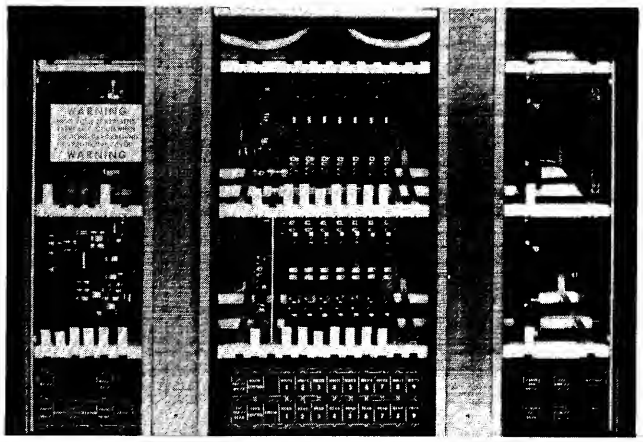


Figure 3-24. Front View of Card Rack

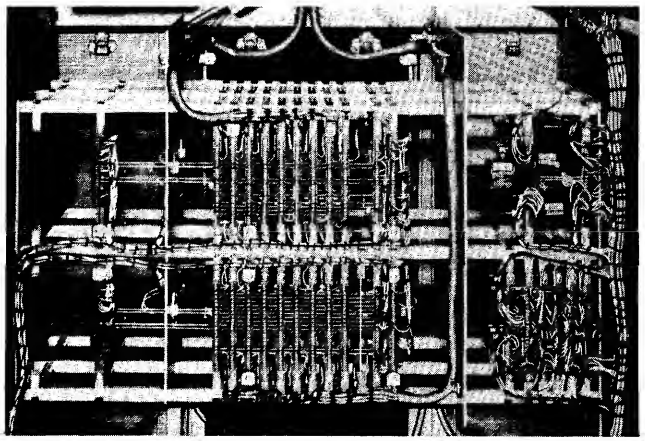


Figure 3-25. Rear View of Card Rack

an upper and lower row of cards. The left-hand compartment, as viewed from the front, houses control and interface circuit cards for the tape unit; the center compartment houses the Data Electronics; and the right-hand compartment houses the extender card, the cards containing power regulator circuits, and the cards containing control switching circuits (on master units). The bulkhead between the Data Electronics and power regulator compartments also serves as a mounting plate and heat sink for power transistors. A card-locating panel at the bottom of the rack indicates the position of each card.

WARNING

The Reel Servo card located behind the protective cover in the Card Rack operates at line voltages. To avoid injury, exercise caution when servicing this section.

3-64. All circuit cards are the size shown in Figure 3-26, and all cards have an ejector lever to facilitate removal from the Card Rack. Connectors are standard 22-position, card edge connectors and are single- or double-sided, depending upon the complexity of the circuit on the card. Between-pin keying is employed to prevent cards from being inserted in the wrong location. Key locations are listed in Table 3-1.

3-65. A double-sided extender card is provided for troubleshooting and servicing the circuit cards. The keying notches are staggered so that it will fit into all the Data Electronics receptacles when inserted in one direction and into all the control and control switching receptacles when turned over and inserted. The arrow adjacent to the word DATA or CONTROL on the extender card should point upward when servicing the corresponding type of card. A small wire hook attached to the extender card

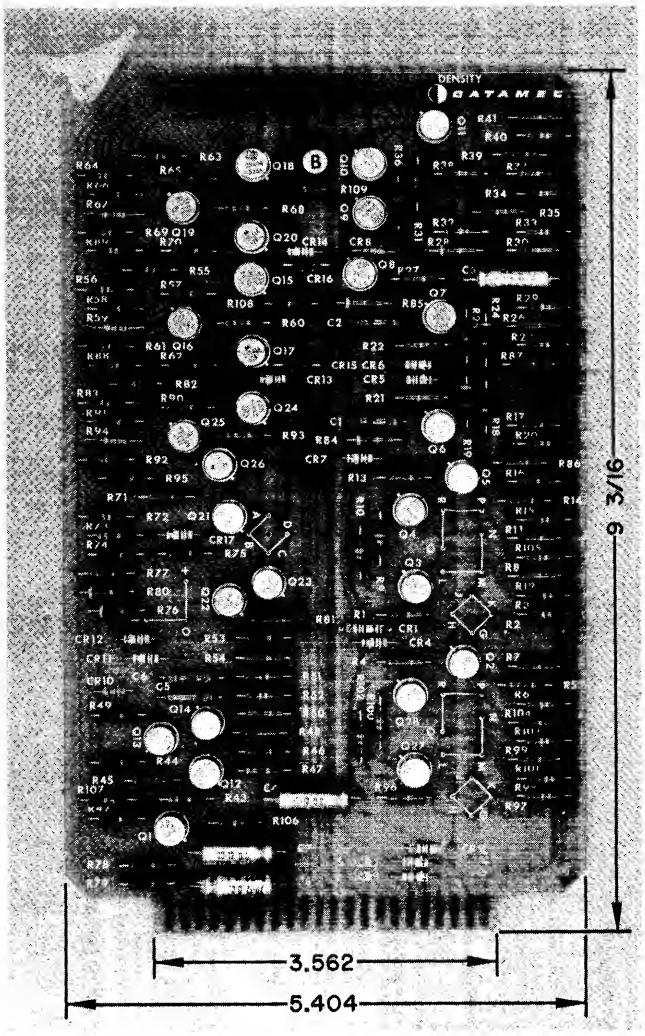


Figure 3-26. Typical Circuit Card

Table 3-1. Circuit Card Connector Keying

CIRCUIT CARD	KEY LOCATION (BETWEEN PINS)	CARD RACK CONNECTOR	EXTENDER CARD SIDE
Relay	2-3	J10	CONTROL
Reel Servo	4-5	J11	CONTROL
Photosense	6-7	J12	CONTROL
Density	8-9	J13	CONTROL
Auto/Local & End-of-Tape	10-11	J14	CONTROL
Rewind	13-14	J15	CONTROL
Load Point	15-16	J16	CONTROL
Drive	17-18	J17	CONTROL
Write Control	1-2	J20	DATA
Write	3-4	J22 to J30	DATA
Read Control	5-6	J33	DATA
Read	7-8	J35 to J43	DATA
Lateral Parity	9-10	J19, J32	DATA
Power Regulator	14-15	J45, J51	DATA
Input (Switcher)	19-20	J47	CONTROL
Output (Switcher)	21-22	J53	CONTROL

can be inserted in a hole in the corner of the circuit card being serviced to keep the card firmly seated in the connector.

CAUTION

To prevent cross-connecting terminals and damaging components on a circuit card during servicing, first insert the circuit card into the Extender card connector, then install the Extender card and attached circuit card in the Card Rack.

3-66. POWER SUPPLY.

3-67. All of the bulky components associated with primary power distribution and raw DC power supplies are located on a single chassis (Figure 3-27) at the bottom rear of the cabinet. Primary power is brought through a standard U-ground connector and channeled to two separate on-off switches, one for the Tape Transport and one for the Data Electronics. These circuits are then divided into separately-fused branches.

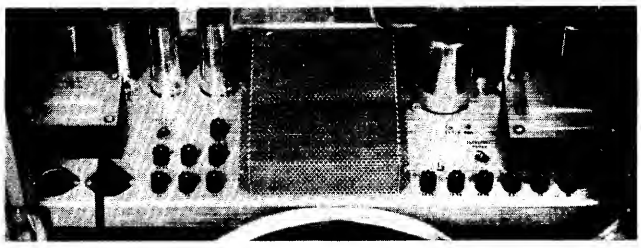


Figure 3-27. Power Supply Chassis

3-68. Transformer T1 feeds rectifier circuits which provide the following supplies for the tape transport: -24 volts DC at 5 amps, -10 volts DC at 0.5 amp, +10 volts DC at 0.5 amp, and -15 volts, unfiltered, at 1 amp. Transformer T2 provides four isolated 16-volt DC, 1.5-amp supplies which are regulated down to 10 volts by the power regulator cards in the Card Rack. T2 also provides a Zener-regulated 16-volt bias supply for the Data Electronics. Power to the tape unit is distributed through barrier terminal strips located along the front edge of the Power Supply chassis.

3-69. CABINET AND COVER DOOR.

3-70. The D-3030 Cabinet is of welded steel construction and serves as the structural framework for the complete tape unit and the protective and decorative housing for the components. Two vertical mounting rails at the front support the Control Panel, Tape Drive Plate, Card Rack, and Vacuum Plate. Horizontal rails at the bottom provide a mounting for the Vacuum Motor Deck and Power Supply. The rear of the cabinet is enclosed by a side-hinged door and a bottom-hinged panel. The latter serves as a mounting plate for input-output connectors and the air outlet assembly. The entire front of the cabinet is protected by a Cover Door assembly which contains two transparent panels and a panel associated with the Control Panel switches and indicators. The door frame is formed from an aluminum alloy extrusion and the transparent panels are acrylic plastic. The lower panel is fixed; the upper panel is counterbalanced and slides down and up for access to the reels and tape threading path. The Cover Door is hinged at the right-hand side and may be opened for cleaning and servicing components. A small catch at the center-left of the cabinet frame holds the door closed and is accessible by lowering the slide panel.

3-71. CIRCUIT OPERATION.

3-72. To describe the electrical and electronic operations performed in the D-3030G-H01 Tape Unit, the various circuits are grouped into three general categories according to function, rather than location, within the unit. The categories are tape handling, control and interface logic and data electronics. Tape handling includes the circuits directly involved with the physical movement of tape. Control and interface logic circuits issue the commands for tape handling and report the operational status of the tape unit. Data electronics concerns all the functions of writing and reading data on tape.

3-73. TAPE HANDLING.

3-74. Three tape handling oeprations are performed by the tape transport: Forward drive, Reverse drive, and Rewind. Starting and stopping the tape unit, however, are performed manually after loading and threading the tape. For references, see the Power Supply schematic diagram and the transport control schematic diagram in Section IV. The latter is a composite schematic diagram which includes the relay and reel servo circuits and various tape transport electromechanical components. Relay contact functions are listed in Table 3-2.

3-75. POWER ON. (Refer to schematic on page 4-1 and the Power Up Flow Chart.) The 117-volt AC power is brought into the Tape Unit through connector J2 on the Power Supply chassis. Power to the unit is normally turned on and off externally as a function of the computer system. The transport power switch, S1, on the Power Supply chassis is provided for convenience during servicing and is normally turned on. When system power is turned on, power is applied to the vacuum motor, transformer T1, and the bridge rectifier circuit for the reel servos. Reel brakes can be released during tape threading by operating the Transport Switch to close BRAKES switch S2, which applies DC power to the brake coils through doides CR11 and CR12.

3-76. START-BRAKES SEQUENCE.

3-77. (Refer to START-BRAKES sequence flow chart and schematics on pages 4-2 through 4-5). After tape is threaded, the transport is started by operating the

Table 3-2. Relay Contact Functions

RELAY	CONTACTS	FUNCTION
K1 (Power Supply)	1, 2, 3 4, 5, 6 7, 8, 9	Energize vacuum transfer solenoid. Transfer power between Cleaning Switch (open) and capstan motor (closed). Energizes Photosense lamp.
K1 Loop Alarm	8, 9, 10 11, 12, 13	Release takeup reel brake for fast rewind. Drop actuator power on long or short loop condition.
K2 Rewind Job	5, 6, 7 11, 12, 13 14, 15, 16	Energize SCR-2 and SCR-3 gates for job and fast rewind. Hold K2 coil energized during rewind recovery period. Hold K7 coil energized during rewind recovery period.
K3 Disable	5, 6, 7 8, 9, 10 11, 12, 13 14, 15, 16	Provide return path for actuator circuit through Cleaning Switch. Supply -24 volts to relay and control circuits. Supply -10 volts to logic cards. Transfer power between Brake release (open) and Reel Servo (closed).
K4 Reel Servo Stop	5, 6, 7	Disable Reel Servo when transport is stopped.
K5 Rewind	5, 6, 7 8, 9, 10 11, 12, 13 14, 15, 16	Supply DC to Q2 (multivibrator) during fast rewind. Energize K7 coil. Release takeup reel brake for fast rewind. Supply DC to Q1 (multivibrator) during rewind jog.
K6 Rewind	5, 6, 7 8, 9, 10 11, 12, 13 14, 15, 16	Transfer SCR-3 gate to Rewind Jog relay K2. Transfer SCR-2 gate to Rewind Jog relay K2. Open SCR-4 gate. Open SCR-1 gate.
K7 Delayed Rewind	5, 6, 7 11, 12, 13 14, 15, 16	Inhibit Stop switch S4 during fast rewind. Drop actuator power during fast rewind. Hold K7 coil energized.
K8 Rewind	5, 6, 7 8, 9, 10 11, 12, 13 14, 15, 16	Energize K5 and K6 coils. Energize vacuum dump solenoid. Transfer Loop Alarm switch VS6 during rewind. Transfer Loop Alarm switch VS5 during rewind.

Transport Switch to close START switch S3, which applies -24 volts through diode CR23 to the coils of relays K1 (Power Supply) and K4. Closing relay K1 starts the capstan motor and energizes the vacuum transfer solenoid to apply vacuum to the chambers. The vacuum causes Vacuum Safety switch VS7 to close and connect the coil of Disable relay K3 to -24 volts through diode CR17 and Start switch S3. Closure of relay K3 energizes the reel servos, and tape is fed into the chambers.

3-78. As tape enters the chambers, Loop Alarm switches VS5 and VS6 close and provide an alternate path around Start switch S3 through diode CR18 to the coil of relay K3. The Transport Switch may then be released. Relays K1 and K4 are held in by an alternate path through a K3 contact and Stop switch S4.

3-79. After the transport has been started, it will continue to operate until vacuum is lost (opening Vacuum Safety switch VS7), a loop alarm sensing hole is crossed by the tape (opening a Loop Alarm switch VS5 or VS6), or the Transport Switch is moved to the BRAKES position (opening Stop switch S4).

3-80. REEL SERVOS. The reel servo system consists of two tape-storing vacuum chambers with two tape-position sensing holes and switches in each chamber, reel motors equipped with solenoid-actuated disc brakes, and motor drive circuits using silicon-controlled rectifiers as switches. When tape is driven in a direction which removes tape from a chamber beyond the upper sensing hole, the corresponding reel is caused to rotate in the direction to feed tape into the chamber. When tape is fed into the chamber so that the tape loop passes the lower sensing hole, the reel is caused to rotate in a direction to

remove tape from the chambers. When the tape loop is in the center section of the chamber between the two sensing holes, the reel motor is stopped and the brakes are applied.

3-81. Rectifiers CR1 through CR4 supply full-wave rectified current to operate the reel motors and brakes. Forward-conducting diodes CR5 and CR6 provide a small shelf, or time delay, between each half-cycle to allow the SCR's to turn off and recover forward-blocking abilities. Each reel motor has two field windings, one associated with each direction of rotation. the windings are energized by SCR's which are gated by the operation of the vacuum switches connected to the chamber sensing holes. Whenever either winding of a motor is energized, power is also fed through a diode to the associated brake coil. Damping diodes CR7, CR8, CR15, and CR16 absorb energy from the collapsing filed of the motor, otherwise current flow would be sustained and the SCR's prevented from turning off after each cycle of power.

3-82. TAPE DRIVE. Tape is driven in a forward or reverse direction by being clamped against one of two rotating capstans by a pinchroller. The clamping action is the result of energizing an actuator through power transistor drive circuits shown on the Drive Circuits schematic diagram. A simplified schematic diagram of an actuator and driver is shown in Figure 3-28.

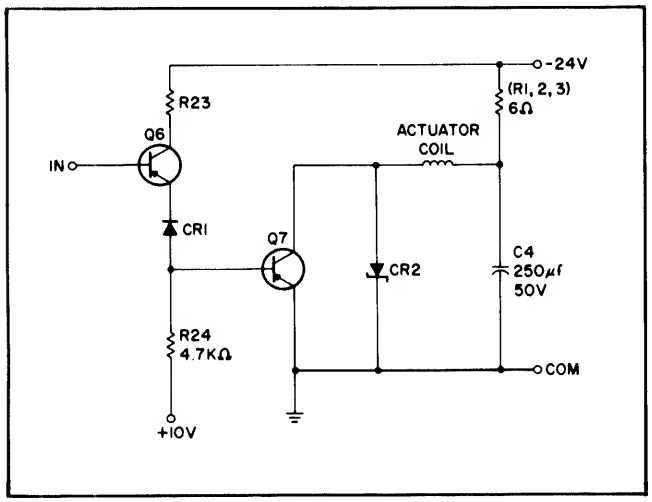


Figure 3-28. Actuator Drive Circuit

3-83. One side of the actuator coil is connected to -24 volts through 6 ohms of resistance (R1, R2, and R3 in the power supply) and the other side to the collector of transistor Q7. When transistor Q7 is off, no current flows, the actuator is open, and capacitor C4 charges to -24 volts. When transistor Q7 is turned on, one side of the coil is clamped to ground, current flows, and a magnetic field builds up in the coil which closes the actuator. The charge on capacitor C4 provides an initial current surge which decreases the pull-in time of the actuator. The steady-state current, reached after 3 or 4 milliseconds, is limited by the 6-ohm resistance and the coil resistance (about 1-3/4 ohms).

3-84. When transistor Q7 is again turned off, current flow ceases, the magnetic field of the coil decays, and the actuator opens. The collapse of the field produces a transient voltage which adds to the supply voltage and appears at the collector of transistor Q7. To prevent damage to the transistor, a 51-volt Zener diode, CR2, limits the voltage between the collector and emitter of the transistor.

3-85. Transistor Q6 serves as a driver for transistor Q7, supplying base current through diode CR1. When transistor Q6 is off, the base of transistor Q7 becomes positively biased by the +10-volt supply through resistor R24. Logic circuits, discussed in paragraph 3-106, provide the input to the base of transistor Q6.

3-86. REWIND. (Refer to Rewind/Unload flow chart.) The automatically controlled Rewind operation consists of removing tape loops from both chambers, driving the supply reel in reverse at full speed to rewind tape from the takeup reel, decelerating both reels when the Tape Pack sensing circuits indicate that about 1/8-inch thickness of tape remains on the takeup reel, loading tape loops into the chambers again, and driving the tape at normal reverse speed to the Load Point tab position, at which point the Rewind operation ceases. Refer to Table 3-2 for the functions of the relay contacts involved in the Rewind operation and the Transport Control Schematic Diagram in Section III.

3-87. During reel-to-reel Rewind, power to the actuator drive circuits is interrupted to prevent an actuator from closing while the tape is moving at high speed. Also, a Fast Rewind response signal is sent to the logic section to indicate that a Rewind operation is being performed.

3-88. The order to initiate and terminate the Rewind operation originated in the logic circuits of the Rewind card and begins with the closing of relay K8. Relay K8, in turn, causes relays K5, K6, and K7 to pull in, resulting in the following actions: normal reel servo operation is suspended, the Loop Alarm turn-off circuit is bypassed, the Loop Alarm switches are connected in parallel to supply -24 volts to transistor Q1, the Vacuum Dump solenoid lessens the chamber vacuum, and power is applied to the jogging multivibrator (transistors Q1 and Q2). As the multivibrator oscillates, it opens and closes relay K2.

3-89. Relay K2 applies alternate bursts of power to the supply and takeup reel motors to jog the tape loops out of the chambers. When the tape loops have cleared both alarm holes, power is removed from transistor Q1, leaving transistor Q2 turned on and relay K2 locked closed to apply full power to the Reverse windings of the supply reel motor. At the same time, Loop Alarm relay K1 drops out and a normally closed contact releases the takeup reel brake. The supply reel pulls tape at high speed from the takeup reel, which is restrained from complete free-wheeling by the drag brake.

3-90. Tape is wound onto the supply reel until the Pack Sense circuit input to the Rewind card logic causes relay K8 to drop out, opening relays K5 and K6. Relays K2 and K7 remain closed for about 1 second after relays K5 and K6 drop out as capacitor C2 discharges into the base of transistor Q2. During the delay, the reels are decelerated and tape loops restored into the chambers.

3-91. The Rewind operation continues as an output of Rewind card transistor Q11 supplies Drive card transistor Q14 to energize the Reverse actuator driver. Tape is driven at normal reverse speed until the Load Point tab is detected by the Photosense head. The Load Point input to the Rewind card resets the Rewind trigger (Q3, Q4, Q5), removing the Reverse drive command.

3-92. PHOTOSENSE AMPLIFIERS. (Refer to Schematic, page 4-6.) The Photosense card contains three photocell amplifier circuits: two circuits connect with the Photosense head assembly photocells which sense the Load Point and End-of-Tape reflective tabs on the tape, and the remaining circuit connects with the tape pack sensing photocell in the Control Panel.

3-93. Referring to the Photosense Amplifiers schematic diagram and using the Load Point circuit as an example, resistors R2 and R3 and the photocell form a voltage divider between +10 volts and ground; and the base of transistor Q1 connects to the junction of the resistors and photocell. The photocell acts as a light-sensitive current source: increasing light causes increasing current. The voltage developed across the resistors and appearing at the base of the transistor will be a function of the light entering the photocell. To accommodate variations in lamps and photocells, an adjustment, R2, is provided. When properly adjusted, the transistor base voltage will be +2.5 volts or more "on-tab" and +0.8 volt or less "off-tab". This voltage can be measured at test point TP1.

3-94. Transistor Q1 is connected as an emmitter-follower and transforms the input voltage from high to low impedance. A low-leakage silicon transistor is used because of the high resistance of the sensing circuit. The output of transistor Q1 is directly coupled to transistor Q2 through resistor R4. Transistors Q2 and Q3 form a conventional Schmitt trigger circuit. When the input is below the trigger level, transistor Q2 is off and transistor Q3 is on. When the input voltage rises above the trigger level, the circuit flips to the opposite state. Transistor Q4 is an inverter and transistor Q5 drives output transistors Q6 and Q7. When a tab is sensed, transistor Q6 is turned off and transistor Q7 connects the output to -10 volts through resistor R20. When a tab is not present, the reverse occurs and the output is clamped to ground by transistor Q6.

3-95. The End-of-Tape sensing circuit is identical to the Load Point sensing circuit. The pack sensing circuit, however, differs only in the input portion: the photocell and resistors are reversed so that the output goes negative when the light source for the cell is interrupted. Since the pack sensing photocell is a low-impedance device, the input emitter-follower is eliminated.

3-96. Transistor Q8 is part of the lamp failure sensing circuit. The photosense lamp current passes through resistor R21 and provides turn-on current for transistor Q8. If the lamp burns out, transistor Q8 turns off and the Lamp Failure line rises to +10 volts.

3-97. CONTROL AND INTERFACE LOGIC.

3-98. Control and interface functions are performed by logic circuits on the Density, Auto/Local and End-of-Tape, Rewind, Load Point, and Drive card. The basic types of logic circuits are few in number; therefore, the basic circuits are described as building blocks and the functions performed when linked together are covered by block diagrams.

3-99. The types of basic circuits used on logic cards include the gate, input trigger, bistable trigger, status line driver, lamp driver, and bus driver. A description and schematic diagram of each follows.

a. Gate: a simple NOR gate, as shown schematically in Figure 3-29, is used extensively for both OR and AND functions. Whe used as an OR gate, the output goes to zero whenever A or B or C is made negative. As and AND gate, the output goes negative whenever A and B and C are zero.

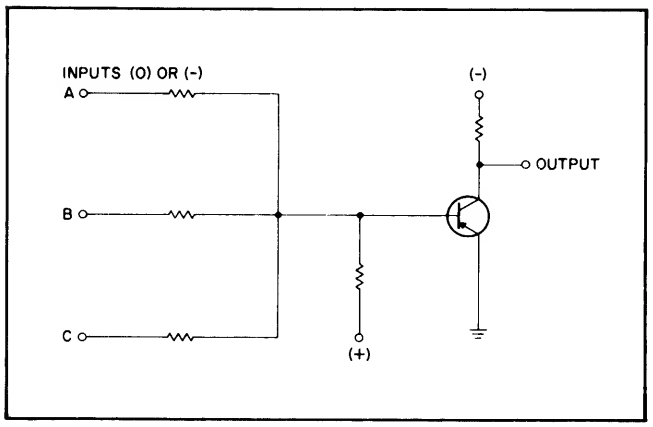
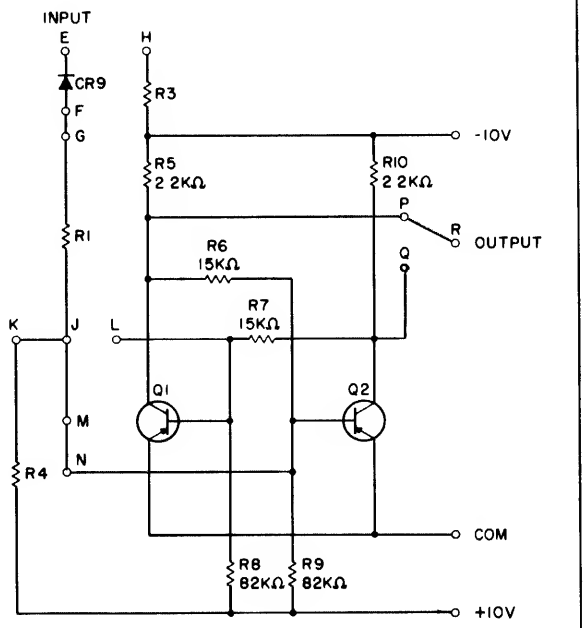


Figure 3-29. NOR Gate Circuit

b. Input Trigger: the input trigger, Figure 3-30, is used as a threshold detector to sense command inputs and convert them to standard logic for subsequent use. Its function is similar to that of a Schmitt trigger, although the circuit more closely resembles a conventional flip-flop that is heavialy biased in one direction. In the absence of an input, the circuit always returns to the same state. It is arranged so that it can be wired to accept positive or negative, true or false input logic. The dotted lines in the figure show the configuration for a negative true input. Transistor Q2 is biased off by resistor R4 connected to +10 volts. To flip the circuit to a true state, a negative voltage must be applied to input terminal E to overcome the positive bias and turn transistor Q2 on. The output, terminal R is taken from the collector of transistor Q1 so that a true input results in a negative output. For negative false input logic, transistor Q2 is biased on by resistor R3,

which connects to input resistor R1 and overcomes the positive bias of resistor R4. For a true input, terminal E must be brought to zero volts (clamped to ground) to allow resistor R4 to turn off transistor Q2. The output is taken from the collector of transistor Q2 so that a true input still produces a negative output. From the connection table in Figure 3-30, it can be seen that positive true or positive false input logic can be made to produce the same output.



INPUT TRIGGER LOGIC CONNECTIONS					
		NEGATIVE TRUE	NEGATIVE FALSE	POSITIVE TRUE	POSITIVE FALSE
CR9	AN.	F	E	E	F
	CATH	E	F	F	E
R3 & R12		NONE	4.7KΩ	15KΩ	15KΩ
R4 & R13		15KΩ	15KΩ	NONE	4 7KΩ
JUMPER WIRES		K TO J	G TO H	H TO K	G TO K
		M TO N	K TO J	M TO L	H TO J
		P TO R	M TO N	P TO R	M TO L
			Q TO R		Q TO R
DASHED LINES SHOWN FOR NEGATIVE TRUE INPUTS					

Figure 3-30. Input Trigger

c. Bistable Trigger: the bistable trigger, Figure 3-31, is a form of flip-flop used as a latching circuit to store an instantaneous command, such as an input pulse, or a momentary operation of a pushbutton. Except for the RC delays incorporated in the cross-coupling, transistors Q1 and Q2 form a conventional flip-flop. The delay is introduced to desensitize the circuit against short spikes of noise. To trigger the circuit, a pulse duration of from 6 to 8 microseconds is required. Transistor Q3 is used to force the trigger in one direction when power is first applied. This is a result of capacitor C3 charging through resistor R11, which momentarily turns on transistor Q3 and clamps the collector of transistor Q2 to ground. The trigger therefore assumes a stable condition (transistor Q2 conducting and transistor Q1 turned off) referred to as Reset. The reverse condition (transistor Q1 conducting and transistor Q2 turned off) is called Set. Various methods are used to Reset and Set the trigger; however, the trigger is generally Set by applying a negative pulse to the base of transistor Q1. Reset is accomplished by pulsing the base of transistor Q2, by momentarily turning transistor Q3 on, or by clamping the collector of transistor Q2 to ground.

d. Status Line Driver: a circuit such as shown in Figure 3-32 is used to provide status indications to the external system controlling the tape unit. The circuit can be strapped for any one of the four types of output logic tabulated in the figure. A true output is obtained when the input to the base of transistor Q1 is zero. Transistor Q1 can also be used as an AND gate, in which case all inputs must be zero to produce a true output. The output transistors (Q2 for a negative output and Q3 for a positive output) switch the output line either to ground through 100 ohms resistance or to the +10-volt supply through 470 ohms resistance.

e. Lamp Driver: Control Panel indicator lamps are turned on and off by the type circuit shown in Figure 3-33. A negative voltage applied to the input terminal turns on transistor Q1, which turns on transistors Q2 and Q3. Transistor Q3 clamps one side of the lamp to common through resistor R8. The other side of the lamp connects to an unfiltered full-wave supply rated at -15 volts RMS. Resistor R8 protects transistor Q3 from an excessive inrush of current when the lamp filament is cold.

f. Bus Driver: a bus driver circuit, Figure 3-34, is used where the fan-out is too great to permit coupling directly from the collector of a NOR circuit or where the load mixture makes it desirable to clamp to both the common and the supply. When the input is made negative, transistor Q1 turns on and supplies base current to turn on transistor Q3. The normal path for base drive to transistor Q2 is through resistors R5 and R6; however, with transistor Q1 turned on, the junction of resistors R5 and R6 is clamped to ground through diode CR1 and transistor Q1. The base of transistor Q2 is slightly positive; therefore, transistor Q2 is turned off. The output is connected to -10 volts through resistor R8, transistor Q1, and diode CR2. When the input is made zero, transistors Q1 and Q3 turn off, transistor Q2 turns on, and the output is clamped to ground. Resistor R8 limits the transient current through transistors Q2 and Q3 during the slight overlap that occurs at the time of swithching.

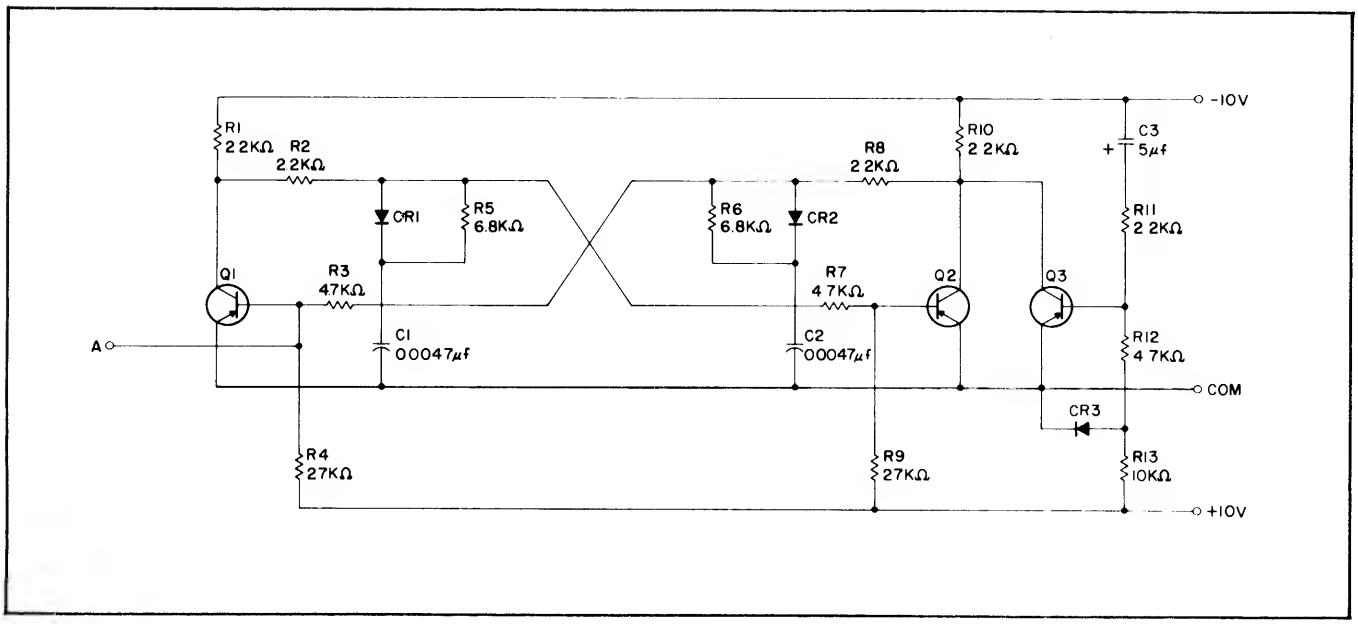
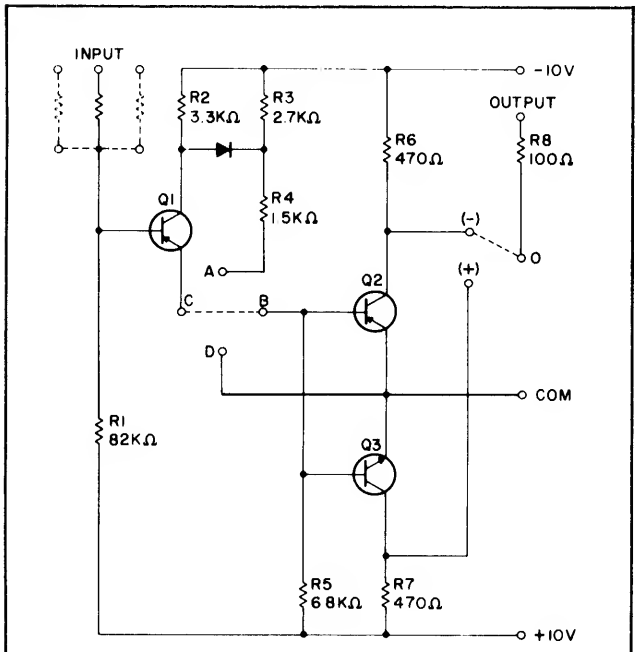


Figure 3-31. Bistable Trigger Circuit



OUTPUT DRIVER LOGIC CONNECTIONS				
	NEGATIVE TRUE	NEGATIVE FALSE	POSITIVE TRUE	POSITIVE FALSE
JUMPER WIRES	B TO C	A TO B	A TO B	B TO C
	O TO (-)	C TO D	C TO D	O TO (+)
		O TO (-)	O TO (+)	
DASHED LINES SHOWN FOR NEGATIVE TRUE OUTPUT				

Figure 3-32. Status Line Driver Circuit

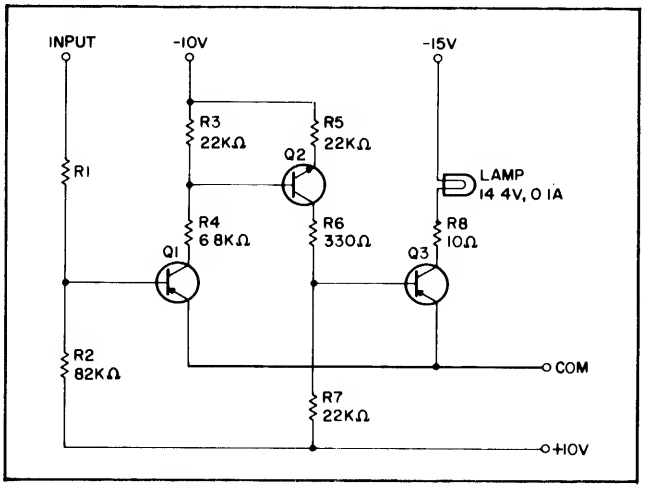


Figure 3-33. Lamp Driver Circuit

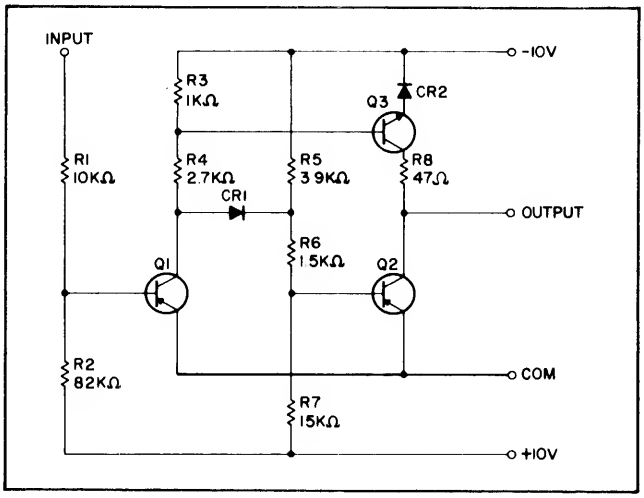


Figure 3-34. Bus Driver Circuit

3-100. A complete logic block diagram of the system is shown in Figure 3-37. The diagram includes all the system inputs and outputs, the control and interface logic cards, the four types of Data Electronics cards, the magnetic head wiring, and the Control Panel pushbuttons and indicators. The blocks in the control and interface logic section of the diagram represent the basic circuits described in paragraph 3-97 and are identified by function and by transistor reference numbers found on the circuit cards and schematic diagrams. (The blocks in the Data Electronics section are also identified by function and transistor reference numbers; however, the circuits involved in the Write, Write Control, Read, and Read Control cards are described in paragraph 3-112.)

3-101. The inputs to each block are labeled according to function and the logic level (voltage) present when the stated condition is true. In general, internal logic levels are ground potential (0) or minus (-). For any line shown as (0), it may be assumed that the opposite state is (-), and vice versa. The exceptions are input and output lines labeled (T) to indicate a "true" level which may be (+), (-), or (0), depending upon the optional strapping of the circuit cards. Further, the Photosense Lamp Fail line operates at a (+) or (0) level. The system "common" line is referred to as being at ground, even though it may not be connected internally to chassis ground.

3-102. A condition with a bar over it means "not true". For example, the Load Point photosense line is shown in Figure 3-35 as an input to two separate blocks, an OR gate and an AND gate. The OR gate in this case makes use of the information that the tape is not positioned at the Load Point. The combination of the tape not at the Load Point AND some other condition YY results in a true output from the AND gate.

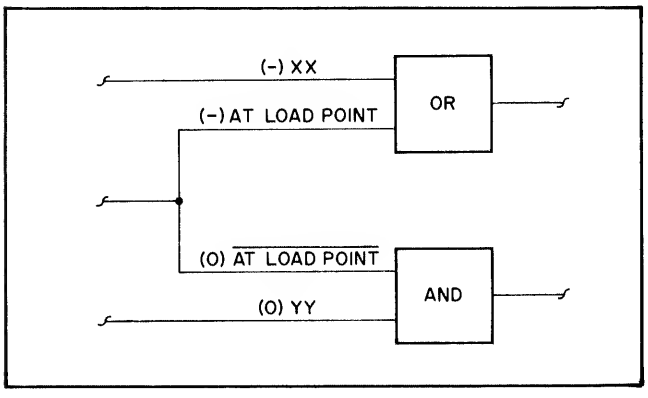


Figure 3-35. Sample Logic Block Diagram

3-103. AUTOMATIC/LOCAL OPERATION. (Refer to Schematic on page 4-15.) Control of the tape unit is transferred between the operator (LOCAL) and the data processing system (AUTO) by the Auto-Local circuits. As shown in Figure 3-37, the Auto-Local trigger is set by the AUTO pushbutton. The trigger energizes the Auto-Local bus driver, the output of which is (0) for AUTO (trigger set) and (-) for LOCAL (trigger reset). The bus controls a number of functions within the system, including the READY status driver (Q11, Q12, Q13). When the input is (0), this driver produces a true output on the READY status line. An inverted output, (-) for AUTO and (0) for LOCAL, is taken from the driver circuit and used as one input to AND gate Q7. Inverted LOCAL (0) is combined with Not FAST REWIND (0) to provide the input to enable the LOAD POINT and REVERSE pushbuttons. The trigger also feeds the AUTO pushbutton lamp driver to illuminate that lamp when the trigger is set. The trigger will be reset by the operation of the LOCAL pushbutton, by the Photosense Lamp Fail circuit, or by an UNLOAD command. The LOCAL pushbutton lamp driver is energized by the AUTO-LOCAL bus so that the lamp is illuminated when the tape unit is in the LOCAL mode of operation.

3-104. DENSITY SELECTION. (Refer to Schematic on page 4-17.) Density is selected manually by a single pushbutton on the Control Panel which actuates a stepping relay. As the relay steps, it connects one of three Density lines to ground. One side of the relay coil connects to -24 volts and the other side to the ENABLE circuit (Q10, Q11, Q12) on the Desnity card through the CHANGE DENSITY pushbutton. The input to the ENABLE circuits is from the AUTO-LOCAL bus: when the input is LOCAL (-), the circuit clamps the pushbutton circuit to ground. Depressing the CHANGE DENSITY pushbutton advances the relay one step whenever the tape unit is in the LOCAL mode. The CHANGE DENSITY pushbutton lamp driver is also controlled by the AUTO-LOCAL bus so that the lamp is illuminated and the switch enabled only when the tape unit is in the LOCAL mode. When one of the density lines (556, for example) is grounded, the associated panel lamp is illuminated. The ground and the AUTO signal supply AND gate Q4 to provide a (-) output to the Data Electronics. The AND gate also energizes the Density 556 status driver (Q5, Q6) to produce a true output on the Density 556 status line.

3-105. FORWARD AND REVERSE DRIVE. (Refer to Schematic on page 4-19.) The pinchroller actuators are controlled by logic circuits on the Drive card. The remote command for Forward drive is applied to the Forward input trigger (Q1, Q2). A true input produces a (0) output which, along with Auto and Not Rewind, is used as an input to AND gate Q3. If all three conditions are true, a (-) output from AND gate Q3 is applied to OR gate Q4. The other input to the OR gate is a signal from the Forward-to-Load Point trigger. The (0) output of Q4 is fed to the actuator drive circuit to close the Forward actuator, provided that the Reverse actuator is not already closed. A cross-interlock circuit between actuator drivers ensures that both actoators can never be closed at the same time, regardless of the input conditions.

3-106. The Reverse logic is similar to the Forward logic. The command passes through a trigger (Q8, Q9) to AND gate Q10. The conditions for an output from Q10 are Reverse, Auto, Not at Load Point, and Not Forward to Load Point. OR gate Q14 provides a true output to the Reverse actuator driver for any of the following conditions: Reverse (from Q10), REVERSE pushbutton, Slow Rewind, or Backward to Load Point. The REVERSE pushbutton, which is active only in the Local mode, also energizes the Reverse lamp driver (Q11, Q12, Q13). An output from AND gate Q10 is also supplied to the Data Electronics to indicate that a command for reverse tape motion is present.

3-107. REWIND. (Refer to Schematic on Page 4-21.) A Rewind operation is initiated by the receipt of a Rewind or Unload command when the tape unit is in the AUTO mode or by depressing the REWIND pushbutton when the unit is in the Local mode. The response of the tape unit is the same in all cases, except that an Unload command also switches the mode from AUTO to LOCAL. When the command is received, the quantity of tape on the takeup reel determines whether a fast (reel-to-reel) or slow (Reverse) rewind will be enacted.

3-108. If a slow rewind is to be performed, the tape is driven in a reverse direction until the Load Point tab is reached. If a fast rewind is to be performed, the operation described in paragraph 3-86 begins. If the Pack Sense circuit malfunctions, fast rewind continues until the Load Point tab is detected. The tape overshoots the tab and stops; tape is loaded into the chambers, then driven forward automatically to the tab in a Load Point search. The tape will always be positioned at the Load Point tab whether a normal fast/slow rewind or abnormal rewind occurs.

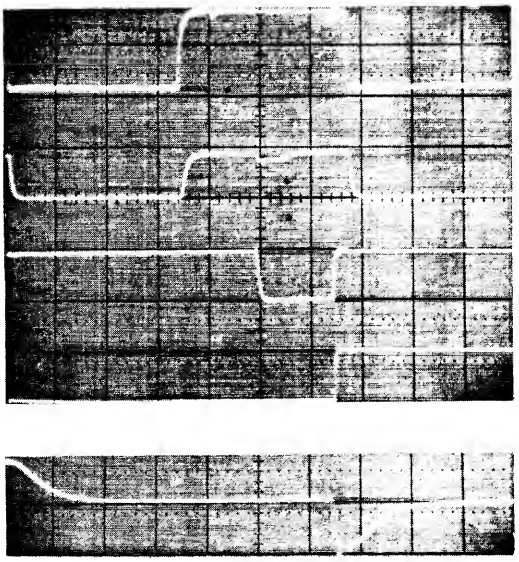
3-109. LOAD POINT SEARCH. (Refer to Schematic on page 4-25 and Flow Chart.) The Load Point search may also be initiated by depressing the LOAD POINT pushbutton when the tape unit is in the Local mode. Load Point status is indicated to the external equipment whenever the tape is positioned at the Load Point and the tape unit is in the AUTO mode. When the tape unit is rewinding or searching for Load Point, Rewind/Load Point Search status is indicated. Details of the logical operation can be traced on the overall logic block diagram, Figure 3-37 and the flow chart.

3-110. WRITE ENABLED. The Write circuits in the Data Electronics are inoperative without a Write Enable Ring installed on the file (supply) reel. The Write circuits are also disabled whenever the tape unit is in the Rewind mode or in a Load Point search operation, even though the reel is equipped with a Write Enable Ring. These interlocks are provided to exclude the possibility of writing data or other extraneous signals under conditions that would destroy data previously recorded on the tape.

3-111. The Write Enable Assembly switch closes when a Write Enable Ring is sensed and provides a grounded input to AND gate Q20. If the Tape Unit is in the AUTO mode and is not rewinding, the output of AND gate Q20 provides a Write Enabled indication to the Write Data Electronics and a Write Enabled status output to the data processing equipment. The status output is dropped when any condition prohibits the operation of the Write Enable circuits. The WRITE ENABLED indicator on the Control Panel, however, is energized only by the Write Enable Assembly.

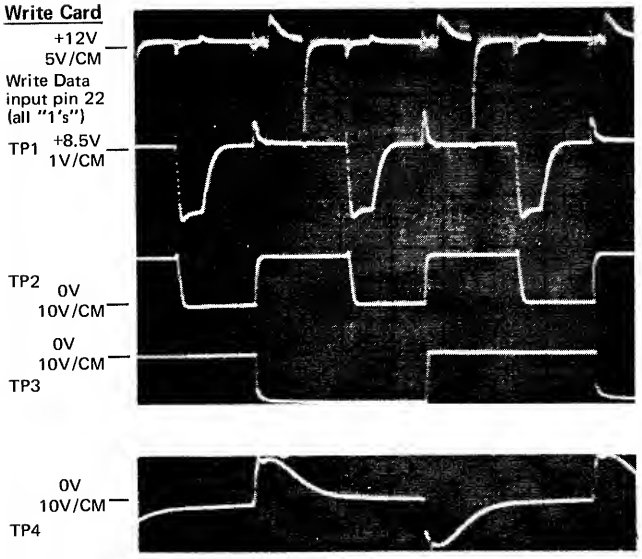
3-112. END OF TAPE. The End-of-Tape indication is initiated whenever the End-of-Tape photoreflective tab passes the Photosense head. A (-) level from the Photosense amplifier sets the EOT trigger (Q14, Q15, Q16) on the Auto-Local and EOT card. The trigger output and the Auto signal feed AND gate Q17, the output of which is applied to the End-of-tape status driver (Q18, Q19). The trigger controls the End-of-Tape lamp driver directly so that the END OF TAPE indicator will be illuminated regardless of the mode of operation of the tape unit. The trigger is reset by a level indicating Rewind status or by operation of the LOCAL pushbutton.

Write Card



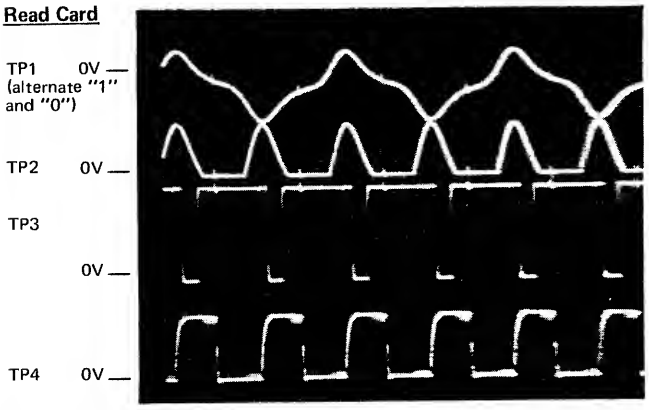
Vert. = 10V/CM
Horiz. = 5 μsec./CM
Sync. = -Top Trace

Write Card



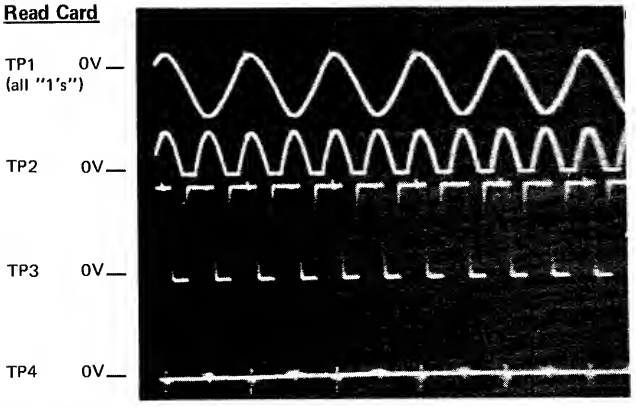
Horiz. = 5 μsec/CM
Sync. = -Top Trace

Read Card

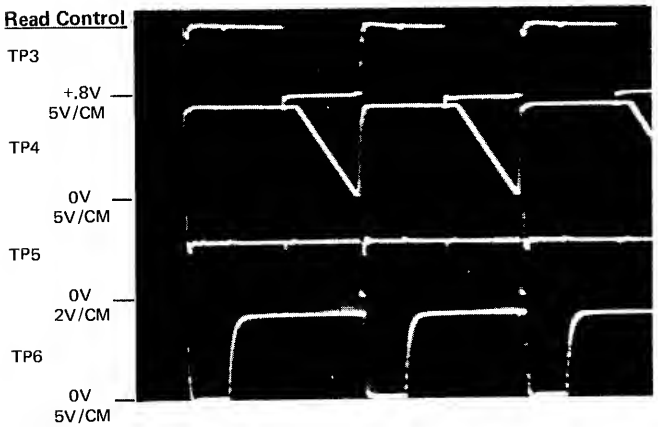


Vert. = 5V/CM
Horiz. = 20 μsec./CM
Sync. = +Top Trace

Read Card

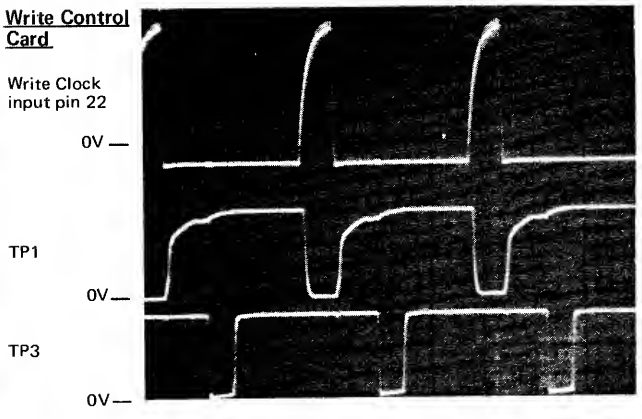


Read Control



Horiz. = 5 μsec./CM
Sync.,= +Top Trace

Write Control Card



Vert. = 5V/CM
Horiz. = 5 μsec./CM
Sync. = +Top Trace

Figure 3-36. Test Point Waveforms

WRITE (J22, J30)

INPUT TRIGGER Q1, 2
STROBE GATE Q3
SKEW DELAY RUNDOWN Q5, 6
WRITE TOGGLE Q7, 8
WRITE DRIVERS Q9, 10
CONSTANT CURRENT GENERATOR Q4
RESET GATE CR25
R55 BAL
R25
-10V
(+F) REGISTER OUTPUT
(+F) WRITE STROBE BUSS
(+F) WRITE RESET BUSS
(-F) WRITE PERMIT BUSS
DATA INPUT
DATA-TRK 1 J4 1 (TO J23)
DATA-TRK 2 J4 2 (TO J24)
DATA-TRK 3 J4 3 (TO J25)
DATA-TRK 4 J4 4 (TO J27)
DATA-TRK 5 J4 6 (TO J29)
DATA-TRK 6 J4 8 (TO J30)
DATA-TRK 7 J4 9 (TO J26)
DATA-TRK 8 J4 11 (TO J28)
WRITE HEAD J8 P8
READ HEAD P9 J9
TRK 1
TRK 2 J23 J36
TRK 3 J24 J37
TRK 4 J25 J38
TRK 5 J26 J39
TRK 6 J27 J40
TRK 7 J28 J41
TRK 8 J29 J42
TRK 9 J30 J43
SHIELD
ERASE

WRITE PARITY (J19)

OUTPUT DRIVER Q20, 21
AND D18, 19
EXCLUSIVE OR D9, 10
HALF-ADDER Q7, 8
HALF-ADDER D1, 2
HALF-ADDER Q3, 4
HALF-ADDER Q5, 6
(0) LOGICAL "1"
PARITY SELECT Q15, 16
GATE PULSE DELAY Q13, 14
BLANKING PULSE Q11, 12
(0) CLOCK PULSE
DATA-TRK 6 J4 5
DATA-TRK 7 J4 7
PARITY SELECT J4 16
(FROM J23)
(FROM J24)
(FROM J25)
(FROM J26)
(FROM J27)
(FROM J28)
(FROM J29)
(FROM J30)

READ (J35, J43)

R12 2041Ω
PREAMP Q4, 5, 6 Q13, 14
FULL WAVE DETECTOR Q15, 16, 17
DIFF & AMPLIFIER Q18, 19, 20
CROSSING DETECTOR Q2
SKEW DELAY RUNDOWN Q22, 23
INPUT REGISTER Q25, 26
OUTPUT REGISTER Q28, 29
OUTPUT DRIVER Q30, 31
CONSTANT CURRENT GENERATOR Q24
STROBE AMPLIFIER Q27
R86 (TRS 5)
R94 (TRS 8)
THRESHOLD INPUT
FWD BUSS
REV BUSS
(+F) "OR" BUSS
(+F) READ STROBE BUSS
(+F) RESET BUSS
(+F) REGISTER OUTPUT
READ PULSE GATE BUSS
READ OUTPUT
DATA-TRK 1
DATA-TRK 2
DATA-TRK 3
DATA-TRK 4
DATA-TRK 5
DATA-TRK 6
DATA-TRK 7
DATA-TRK 8
DATA-TRK 9

READ PARITY (J32)

HALF-ADDER D1, 2
HALF-ADDER Q3, 4
HALF-ADDER Q7, 8
HALF-ADDER Q5, 6
PARITY SELECT Q15, 16
EXCLUSIVE OR D9, 10
PARITY INHIBIT Q17
AND Q18, 19
OUTPUT DRIVER Q20, 21
BLANKING PULSE Q11, 12
GATE PULSE DELAY Q13, 14
(JUMPER CARD)
PARITY SELECT
PARITY ERROR

WRITE CONTROL (J20)

WRITE CLOCK J4 11
WRITE RESET J4 12
WRITE PERMIT J4 13
CLOCK INPUT
WRITE RESET INPUT
WRITE PERM.T INPUT
(PARITY CLOCK OUTPUT)
INPUT TRIGGER Q1, 2
INPUT TRIGGER Q7, 8
INPUT TRIGGER Q10, 11
CLOCK DELAY M.V. Q3, 4
RESET DRIVER Q9
PERMIT GATE D12, 13
STROBE GENERATOR Q5, 6
ERASE HEAD DRIVER Q15
.1M-BIT
WRITE ENABLE
WRITE STROBE BUSS
WRITE RESET BUSS
COMMON
ERASE HEAD CURRENT
WRITE PERMIT BUSS
TB3 20
TB2 2

READ CONTROL (J33)

(+F) READ THRESHOLD BUSS
(-F) FWD BUSS
(-F) REV BUSS
(+F) READ RESET BUSS
(+F) READ STROBE BUSS
(+F) READ "OR" BUSS
(+F) READ PULSE GATE BUSS
"TRIGGER INPUT"
STROBE GENERATOR Q24
4 ax READ CLOCK GENERATOR Q25, 26
THRESHOLD DRIVER Q32, 33
FWD-REV DRIVERS Q29, 30, 31
RESET DRIVER Q15
CHAR GATE GEN Q6 THRU 18, 21, 23
CLOCK OUTPUT DRIVER Q27, 28
(-F) READ/WRITE THRESHOLD INPUT
INPUT TRIGGER Q13, 14
DENSITY SELECT LOGIC Q20, 22
(-F) REVERSE INPUT
READ RESET INPUT
(-F) 556 DENSITY INPUT
(-F) 800 DENSITY INPUT
READ CLOCK OUTPUT
CLOCK
READ RESET
TB3 21
TB2 3
TB3 23
TB3 24
TB2 4
TB2 5

AUTO
PHOTOSENSE LAMP FAILURE
-10V RESET
END OF TAPE PHOTOSENSE
LOCAL
FAST REWIND RESPONSE
LOAD POINT PHOTOSENSE
UNLOAD INPUT
REWIND INPUT
REWIND
REWIND PACK SENSE

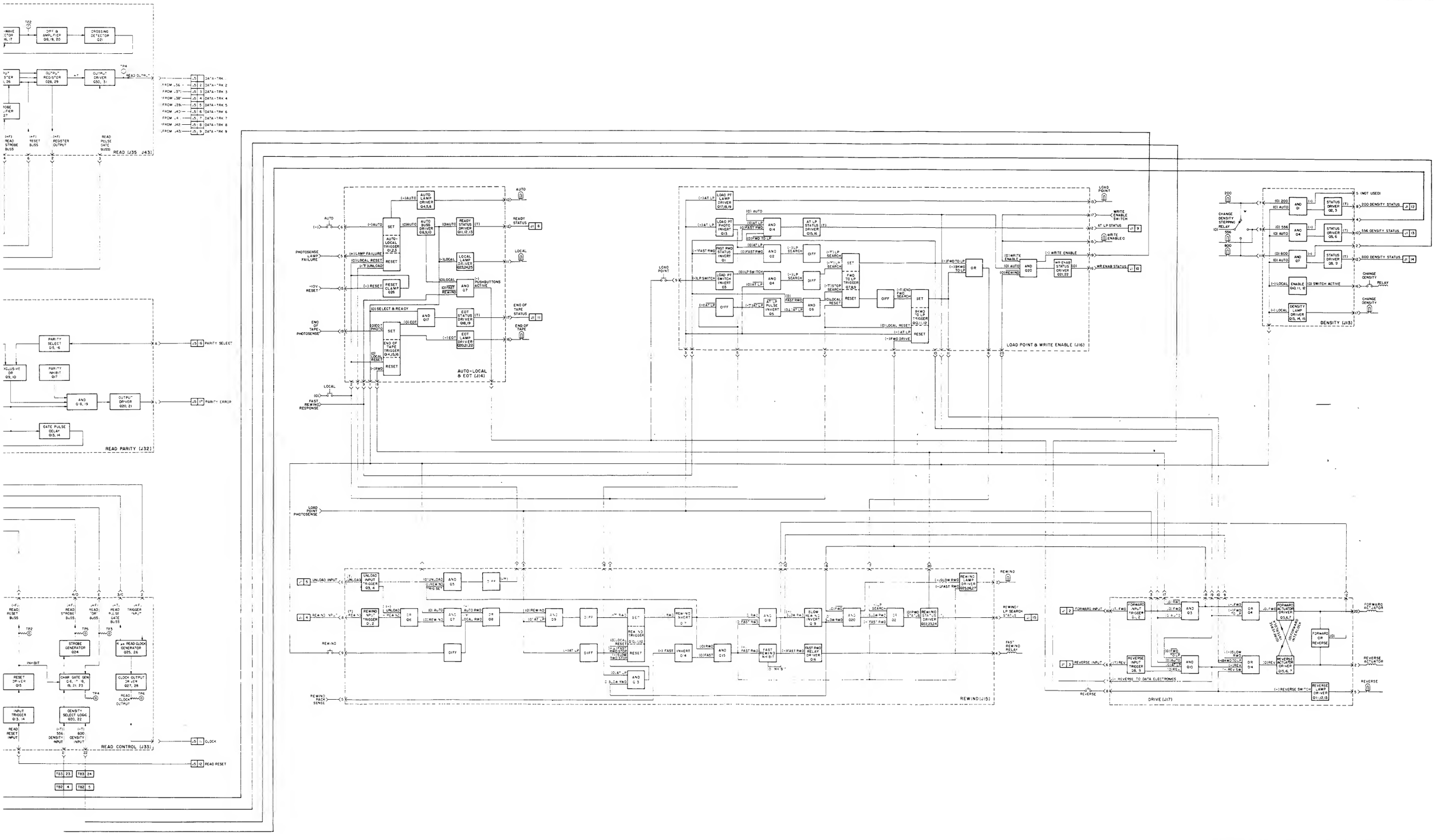


Figure 3-37. System Logic Block Diagram

3-113. DATA ELECTRONICS.

3-114. The Data Electronics consists of nine Write cards, a Write Control card, nine Read cards, and a Read Control card located in the Card Rack. Also included are Read and Write Power Regulator cards to supply +10 volts DC and -10 volts DC to the Read and Write circuits. A Parity Jumper card is inserted in the Lateral Parity card location. In the following paragraphs, the operation of each type of card is briefly described. For details of the circuits, see the schematic diagram for each card in Section IV.

3-115. WRITE CARDS. (Refer to Schematic on page 4-25.) The nine Write cards are identical to one another and are all controlled by the Write Control card. The cards accept 9-channel parallel data, one channel per card, convert the data to NRZI form, and drive the nine Write heads to record the data on tape. The operation of a typical Write card is shown in Figure 3-38, a block diagram of the Write Card schematic diagram. The positive true input to the card, pin 22, feeds an input trigger (Q1, Q2), the output of which varies between ground and a positive level and can be checked at test point TP1. The trigger supplies a positive false output to pin 21, the Register output, and the input to the strobe gate, Q3. If the strobe gate is enabled by the input from the input trigger, the positive-false Write Strobe (Write Clock) input (pin 19) from the Write Control card causes the strobe gate to generate narrow positive-going pulse to start the skew delay rundown by turning off Q5 and Q6. The rundown (Q5, Q6) operates from a constant current generator, Q4, which supplies capacitor C7. The skew delay ensures that the recorded bit alignment will be within tolerances for higher bpi densities. As the rundown circuit drops from about +9.5 volts to ground, it creates the skew time delay which can be checked at test point TP2. At the end of the delay, Q5 and Q6 snap on again and generate a sharp positive-going pulse to the write toggle (Q7, Q8). Depending upon the state of the write toggle, Q7 will be turned off and Q8 turned on (or vice versa) through a group of steering diodes. The write toggle must be enabled by a negative-false Write Permit (Write Enable) input (pin V). The operation of the write toggle can be checked at test point TP3. The write toggle is sent to the write drivers (Q9, Q10) and to the reset gate (CR23). The write drivers supply the associated Write head track (checked at test point TP4) to write a logical "one" or "zero", corresponding to the input signal at pin 22, on the tape. Balance adjustment resistors in the write drivers circuit compensate for any asymmetry characteristics in the individual Write heads. A negative-false Write Reset command from pin 17 causes another skew delay rundown to reset the write toggle. If the write toggle is in a set condition, the Write Reset pulse switches it to a reset condition, causing another one to be written.

3-116. WRITE CONTROL CARD. (Refer to Schematic on page 4-27.) The Write Control card supplies a Write Strobe (Write Clock) pulse to the Write cards, when writing is permitted and enabled, to cause all the Write card data to be written on tape within the alignment tolerances required for 800 bpi density. It also enables the Write Permit buss from a Write Permit (Write Enable) input, which is a provision for external on-off control of all head current. By enabling the Write Reset bus upon receipt of a Write Reset input, the card also causes all head current to switch to a common direction for writing an inter-record gap, or other gaps, on tape. The operation of the Write Control card is shown in Figure 3-39, a block diagram of the Write Control Card schematic diagram.

3-116. To generate the Write Strobe output to the Write cards, a positive-false Clock input on pin 22 is received by an input trigger (Q1, Q2). The output of the trigger, checked at test point TP1, drives the

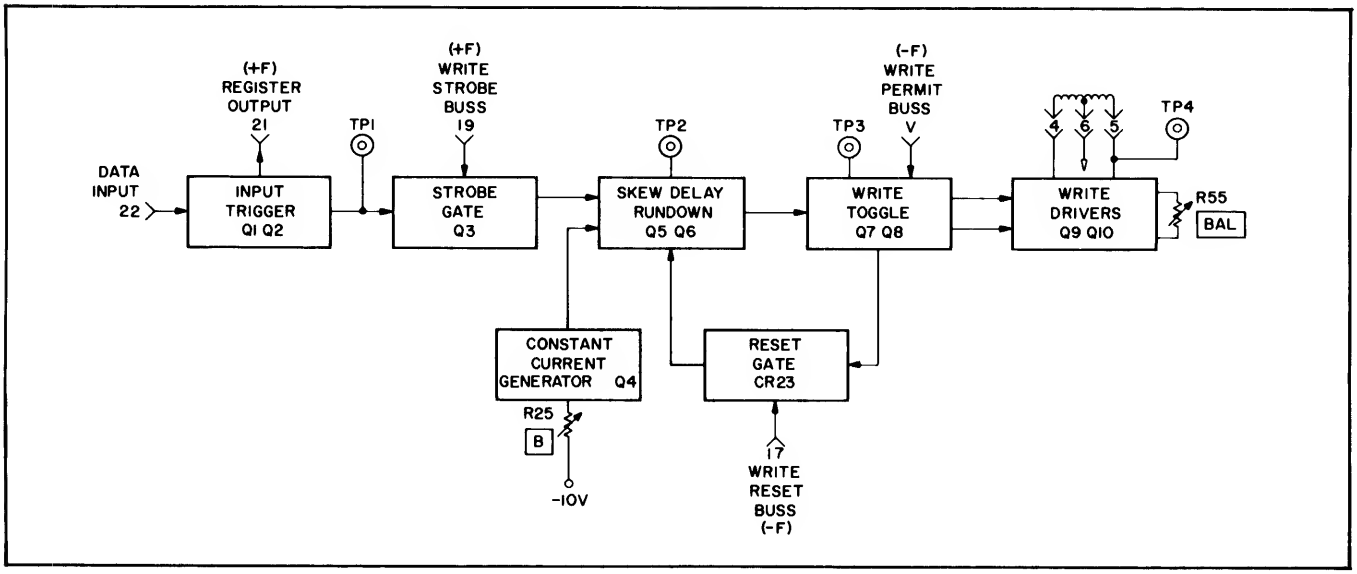


Figure 3-38. Write Card Logic Block Diagram

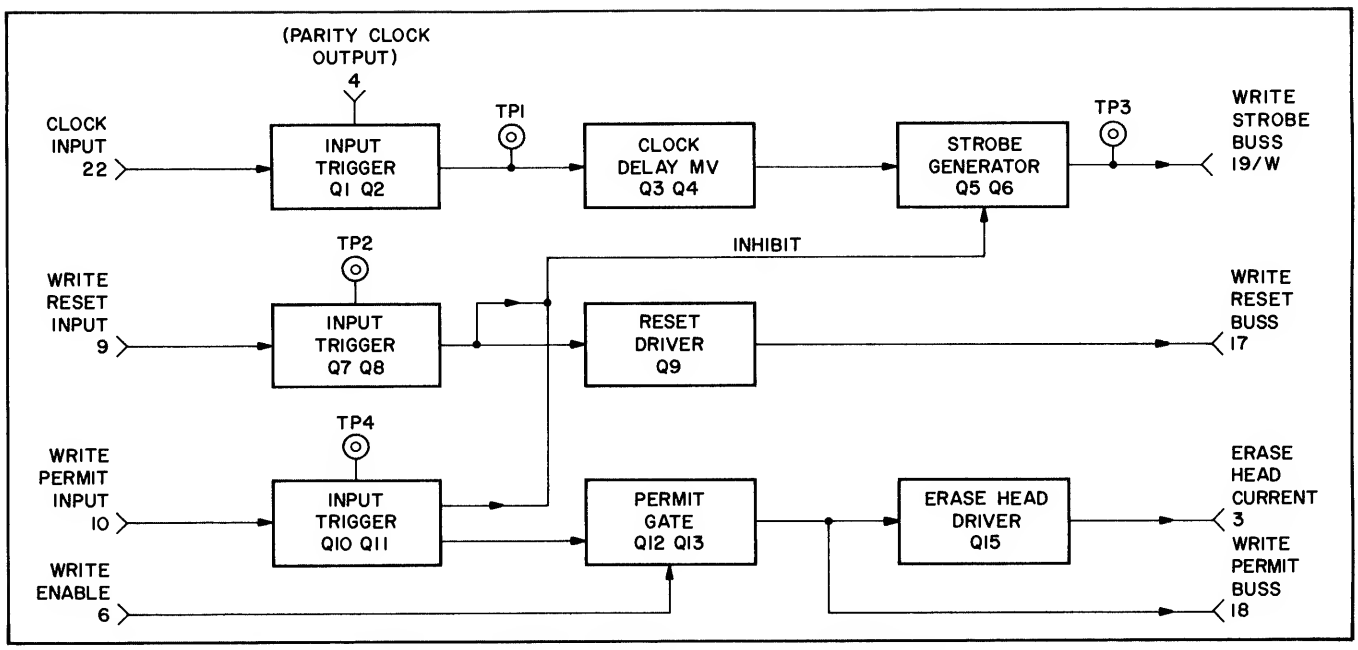


Figure 3-39. Write Control Card Logic Block Diagram

one-shot clock delay multivibrator (Q3, Q4). After a nominal 4-microsecond delay, the clock delay multivibrator provides an input to start the strobe generator (Q5, Q6). If an inhibit signal from the Reset input trigger or the Write Permit input trigger is not present, the Write Strobe bus is enabled momentarily by the strobe generator, the output of which can be checked at test point TP3. A Write Permit input from the external control equipment is supplied at pin 10 to the Write Permit input trigger (Q10, Q11). The output of the trigger, checked at test point TP4, is one of two inputs to the Permit AND gate (Q12, Q13). The other input (pin 6) derives from the Write Enable circuits (Write Enable Ring installed and tape unit in the AUTO mode and not rewinding). When both inputs are present, the Permit gate enables the Write Permit bus (pin 18) to supply current to the Erase head on pin 3. If a Write Permit input is not present, an inhibit signal is sent to the strobe generator to disable its operation. A Write Reset input on pin 9 from the external equipment enables the Write Reset bus (pin 17) through the Reset input trigger (Q7, Q8) and the Reset driver (Q9). The output of the Reset input trigger, checked at test point TP2, also sends an inhibit signal to the strobe generator to disable it from operating while the Write Reset bus is enabled.

3-118. READ CARDS. (Refer to Schematic on page 4-29.) The nine Read cards amplify the outputs of the nine Read heads, detect the recorded "one" bits, and store the "one" bits temporarily in an output register. The Read cards are controlled by the Read Control card, and all Read cards are identical in configuration and operation. The operation of a typical Read card is shown in Figure 3-40, a block diagram of the Read Card Schematic Diagram.

3-119. The impulses from the Read head are fed into a preamplifier (Q4, Q5, Q6, Q13, Q14), the output of which can be sampled at test point TP1, and a full-wave detector (Q15, Q16, Q17). A Threshold input (pin U) to the detector circuit serves to change the detection level from a normal 20 percent of full pulse amplitude to 40 percent during a Read-After-Write operation. The output of the detector is a rectified signal, checked at test point TP2, which becomes the input to a differentiator and amplifier (Q18, Q19, Q20). These circuits detect the "one" bits at the time of their pulse peaks to reduce the time displacement error caused by pulse amplitude variations. A crossing detector (Q21), operating from the output of the amplifier, provides a pulse to the skew delay rundown (Q22, Q23). The rundown draws current from a constant current generator (Q24) which has a trimming adjustment (R86 and R94) for forward and reverse tape motion. as determined by a Forward (pin K) or Reverse (pin L) input from the control logic circuits. The skew delay rundown compensates for variations in pulse alignment on tape. At the end of the delay rundown, the detected "one" bit enters an input register (Q25, Q26). The input register supplies an input to the OR bus (pin 5) for the Read Control card character gate. A positive-false pulse from the Read Strobe bus (pin 4) is detected by the strobe amplifier (Q27), which causes the input register to shift its contents to the output register. The output register positive-true signal enables the output driver which provides the positive-false Read output on pin 1. A positive-false signal on the Reset bus (pin 6) resets the register.

3-120. READ CONTROL CARD. (Refer to Schematic on page 4-31.) The Read Control card generates several enable signals to the Read Cards upon receipt of command signals from the control logic circuits. The operation of the Read Control card is shown in Figure 3-41, a block diagram of the Read Control Card schematic diagram.

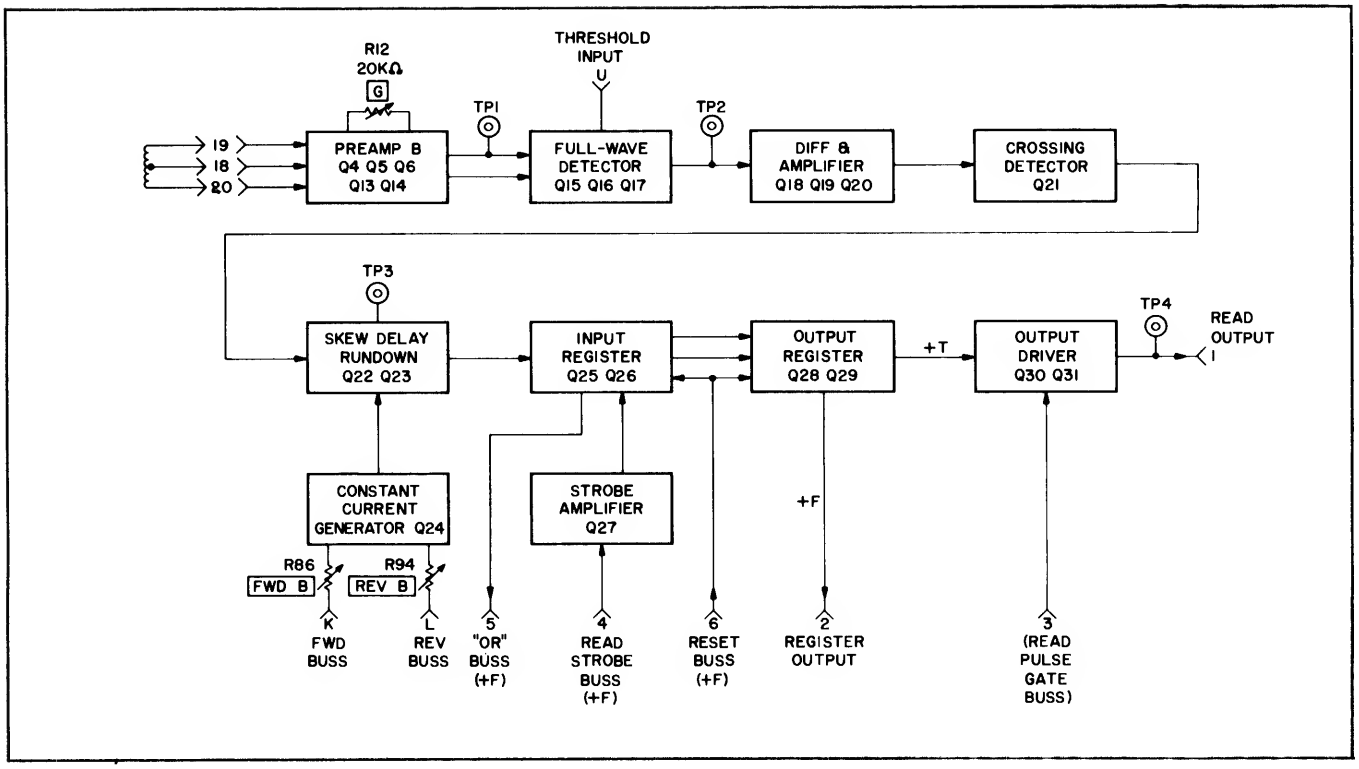


Figure 3-40. Read Card Logic Block Diagram

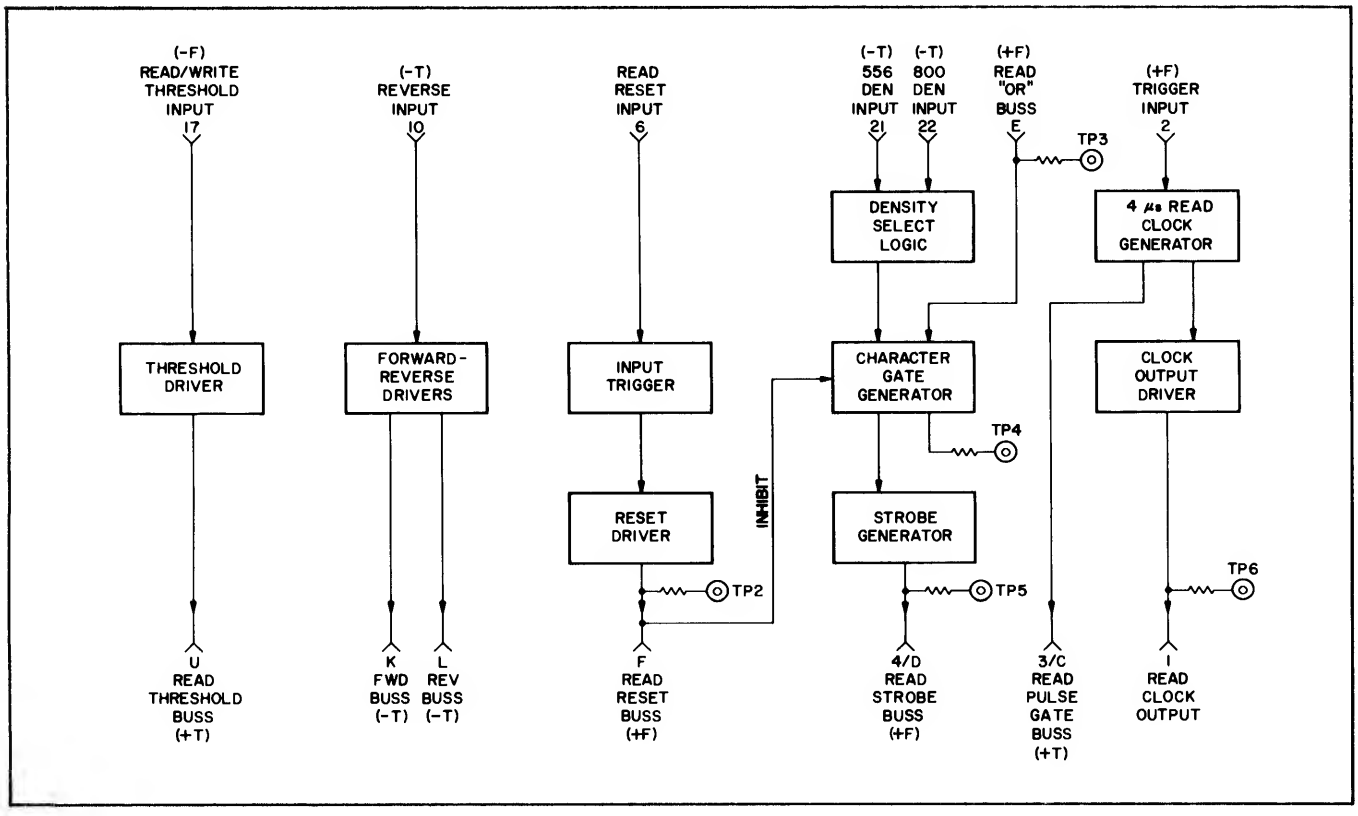


Figure 3-41. Read Control Card Logic Block Diagram

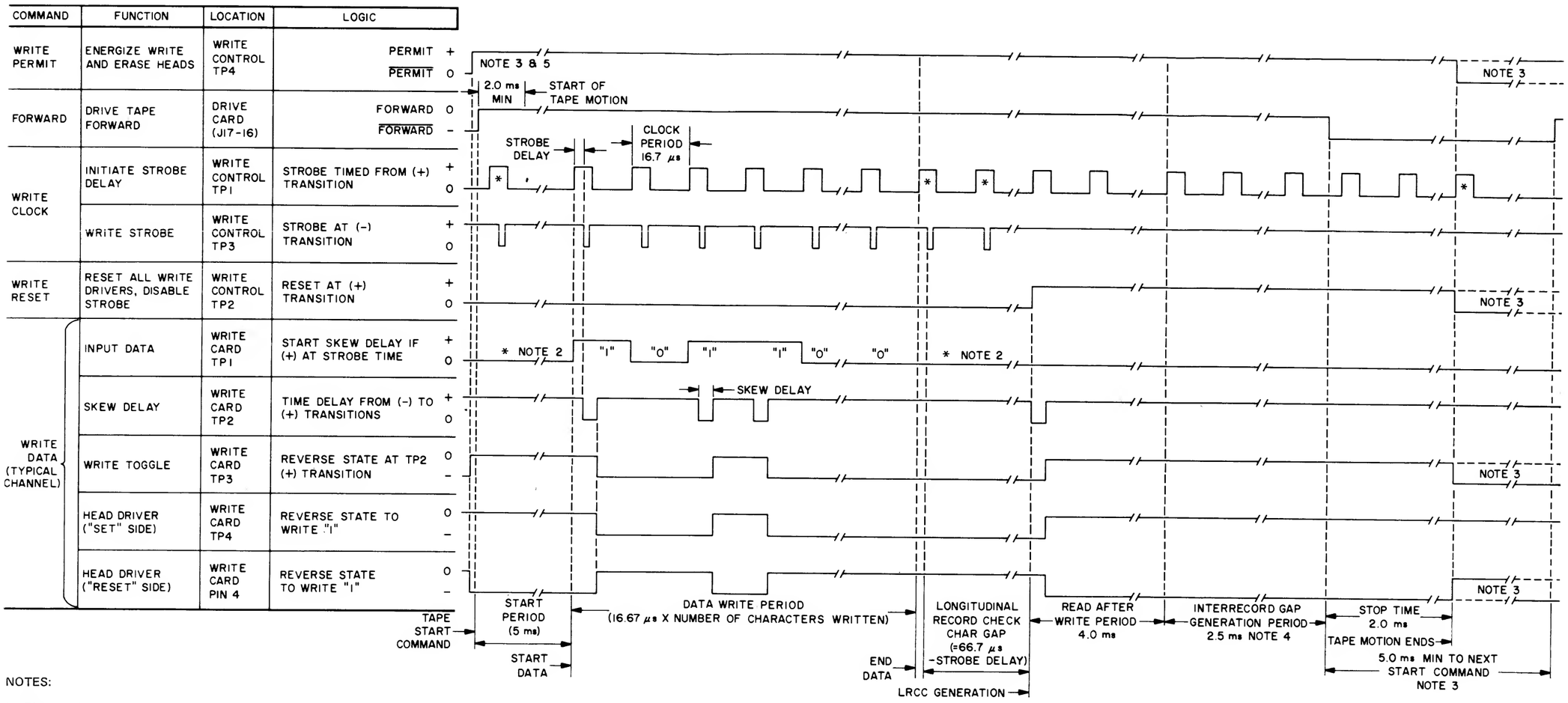
3-121. During a Read-After-Write operation, a negative-false Threshold input (pin 17) energizes the threshold driver to enable the Threshold bus (pin U), which changes the detection level of the Read cards. A negative-true Reverse input (pin 10) to the forward-reverse drivers causes either the Forward bus (pin K) or Reverse bus (pin L) to be enabled to set appropriate delay circuits on the Read cards. A negative-true density input on pin 21 (Density 556) or pin 22 (Density 800) to the density select logic provides one input to the character rage generator. The addition of a second input, a positive-false OR bus input on pin E, energizes the character gate generator. At the end of the character gate time delay, the strobe generator is energized: the strobe pulse momentarily enables the Read strobe bus for all the Read cards. A negative-true Read Reset input on pin 6 energizes the Read Reset bus (pin F) through the Reset input trigger and Reset driver. This signal resets all the Read Card registers and provides an inhibit signal to the character gate generator to disable it during a Reset operation. A positive-false Trigger on pin 2 energizes the Read Clock generator to provide a nominal 4-microsecond pulse to the Read Pulse Gate bus (during pulse operations) and energizes the Clock Output driver to provide a positive-false Read Clock output on pin 1.

Note

If the tape unit is being operated with a Write Enable Ring and if it is desired, for some reason, to disable the Write process for a short time, disengaging the Write Control card from its rack connector prohibits the Write function. Both the Write Control card and the Write Power Regulator card may be disengaged together for this purpose; however, disengaging the Write Power Regulator card alone is not advised: generation of a spurious threshold signal to the Read cards will result.

3-122. TIMING. Typical overall timing of the Write and Read Data Electronics operations are shown in Figures 3-42 and 3-45. The sequences shown pertain to a standard clocked level system operating in the AUTO mode at a tape speed of 75 ips and bit-packing density of 800 bpi. Detailed timing sequences of the internal operations of Write and Read data cards are shown in Figure 3-44 (for systems without Parity) and Figure 3-45 (for systems with Parity).

COMMAND	FUNCTION	LOCATION	LOGIC
WRITE PERMIT	ENERGIZE WRITE AND ERASE HEADS	WRITE CONTROL TP4	PERMIT + $\overline{\text{PERMIT}}$ 0
FORWARD	DRIVE TAPE FORWARD	DRIVE CARD (J17-16)	FORWARD 0 $\overline{\text{FORWARD}}$ -
WRITE CLOCK	INITIATE STROBE DELAY	WRITE CONTROL TP1	STROBE TIMED FROM (+) TRANSITION + 0
	WRITE STROBE	WRITE CONTROL TP3	STROBE AT (-) TRANSITION + 0
WRITE RESET	RESET ALL WRITE DRIVERS, DISABLE STROBE	WRITE CONTROL TP2	RESET AT (+) TRANSITION + 0
WRITE DATA (TYPICAL CHANNEL)	INPUT DATA	WRITE CARD TP1	START SKEW DELAY IF (+) AT STROBE TIME + 0
	SKEW DELAY	WRITE CARD TP2	TIME DELAY FROM (-) TO (+) TRANSITIONS + 0
	WRITE TOGGLE	WRITE CARD TP3	REVERSE STATE AT TP2 (+) TRANSITION 0 -
	HEAD DRIVER ("SET" SIDE)	WRITE CARD TP4	REVERSE STATE TO WRITE "1" 0 -
	HEAD DRIVER ("RESET" SIDE)	WRITE CARD PIN 4	REVERSE STATE TO WRITE "1" 0 -



NOTES:

1 Diagram shows typical timing of clocked level system for writing one or several IBM-compatible record blocks in Automatic mode at 75 ips, 800 bpi. Waveforms shown are symbolic; refer to Section V for actual waveforms and detailed timing.

2 When Clock train needs to be provided only during Data Write period. If present outside of Data Write period, Data inputs must be false whenever Write Reset is false and Write Permit is true. For systems with internal Lateral Parity generation and/or internal LRCC, refer to text.

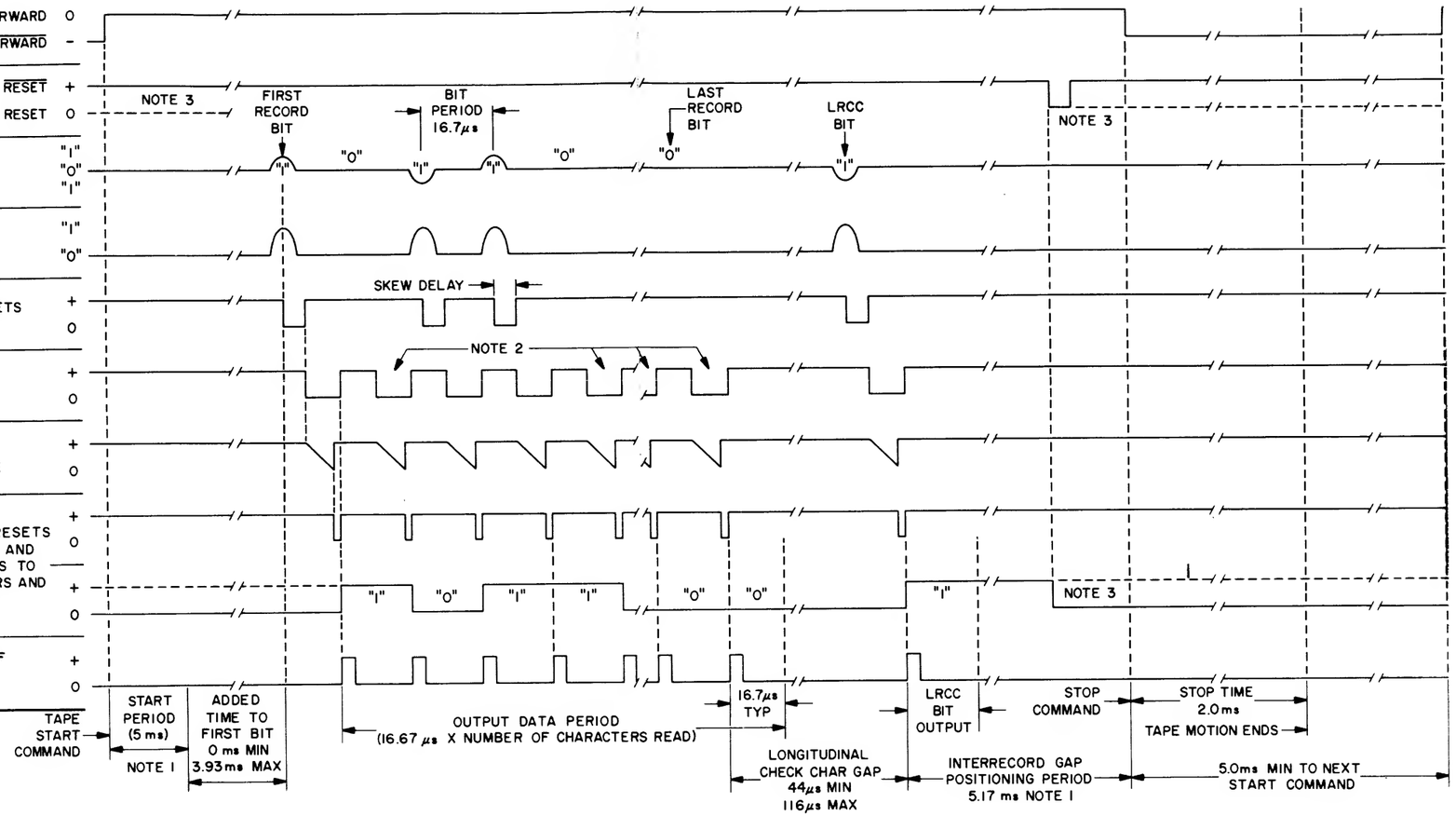
3 Write Permit must be true at least from start of tape motion to end of tape motion. If next record block is to be written immediately, Write Permit may be maintained true and Write Reset may be maintained true until beginning of following Data Write period.

4 Record Gap length is equal to: Tape Start distance + Tape Stop distance + Write-to-Read head gap distances + (Record gap generation period X Tape Speed).

5 Whenever Write Permit is made false with tape standing still, noise will be written; if Write Permit is then made true before tape motion begins, the noise will be erased. However, if next tape motion is for a Read operation (such as "backspace, read"), the noise will remain and may or may not be erased by next Write operation performed.

Figure 3-42. Write Data Electronics Timing Diagram.

COMMAND	FUNCTION	LOCATION	LOGIC	
FORWARD	DRIVE TAPE FORWARD	DRIVE CARD (J17-16)	FORWARD	0
			$\overline{\text{FORWARD}}$	-
READ RESET	HOLD READ CARD INPUT AND OUTPUT REGISTERS FALSE	READ CONTROL TP2	$\overline{\text{RESET}}$	+
			RESET	0
READ SIGNALS	PREAMP SIGNAL OUTPUT (TYPICAL)	READ CARD TP1	POSITIVE AND NEGATIVE PEAKS REPRESENT "1"'S	"1" "0" "1"
	FULL-WAVE DETECTOR OUTPUT	READ CARD TP2	POSITIVE PEAKS REPRESENT "1"'S	"1" "0"
	SKEW DELAY	READ CARD TP3	(+) TRANSITION SETS INPUT REGISTER	+ 0
	READ "OR" BUSS (+ FALSE)	READ CONTROL TP3	"OR" BUSS TRUE WHILE ANY INPUT REGISTER SET	+ 0
	CHARACTER GATE	READ CONTROL TP4	(+) TRANSITION TRIGGERS STROBE	+ 0
	READ STROBE	READ CONTROL TP5	(+) TRANSITION RESETS INPUT REGISTERS AND SHIFTS CONTENTS TO OUTPUT REGISTERS AND OUTPUT DRIVERS	+ 0
	DATA OUTPUT (+ TRUE SHOWN)	READ CARD TP4		+ 0
	CLOCK OUTPUT (+ TRUE SHOWN)	READ CONTROL TP6	(+) TRANSITION OF STROBE STARTS SINGLE-SHOT	+ 0



NOTES:

1 Diagram shows typical Read-only timing of clocked level system for reading IBM-compatible tape at 75 ips, 800 bpi. Timing accommodates Start and Stop distance tolerances and Inter-record Gap length tolerance. For Read-After-Write operation, IRG positioning period becomes 2.5 ms and time from end of start period to first Data bit becomes 4.0 ms. Waveforms shown are symbolic; refer to Section V for actual waveforms and detailed timing.

2 Read "OR" signals shown are initiated by bits in other tracks.

3 Output registers hold last character read until Read Reset command is given (optional). Read Reset must be false before first record bit and until after LRCC output.

Figure 3-43. Read Data Electronics Timing Diagram

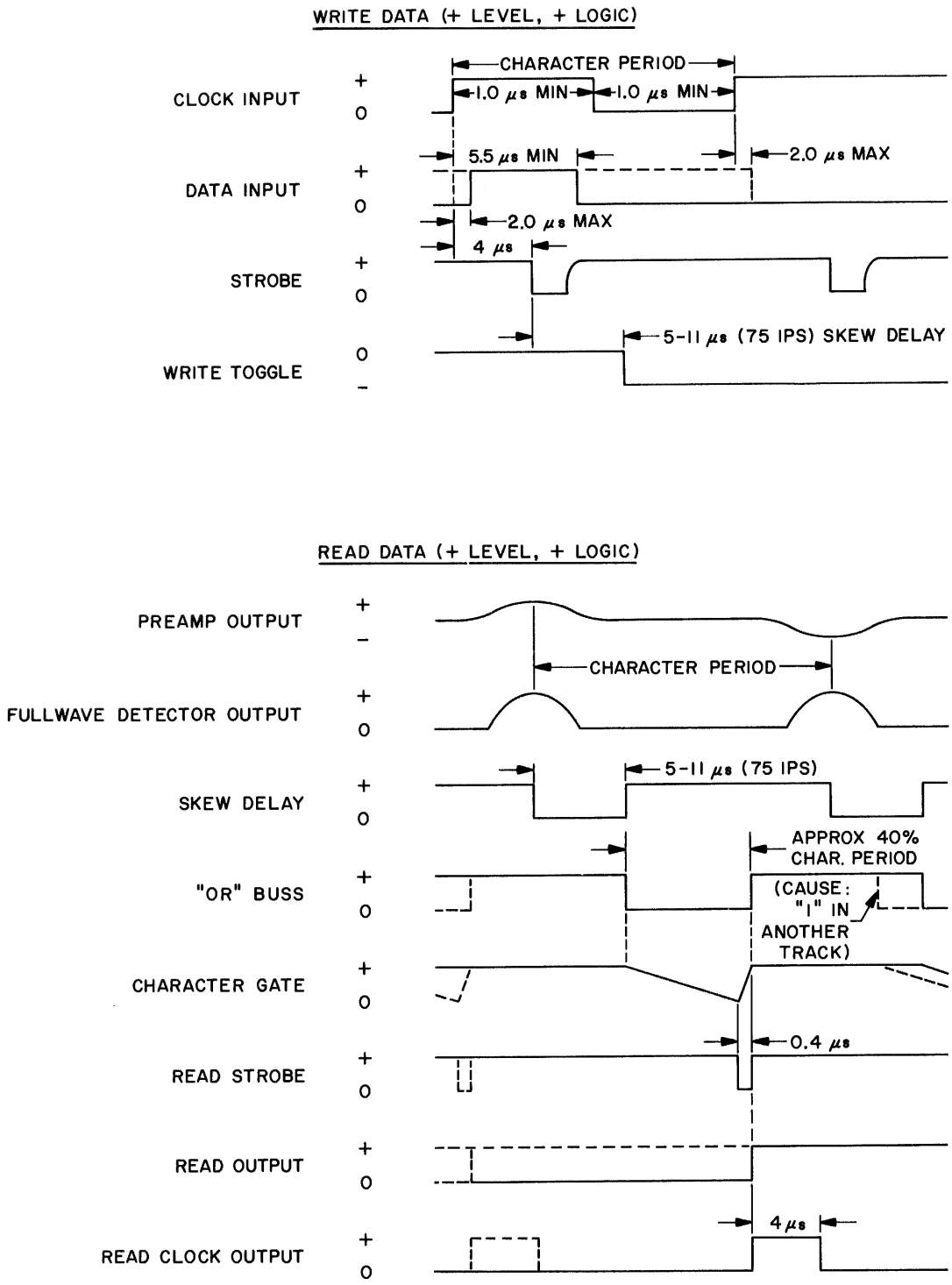


Figure 3-44. Detailed Timing Diagram for Write/Read Level System without Parity

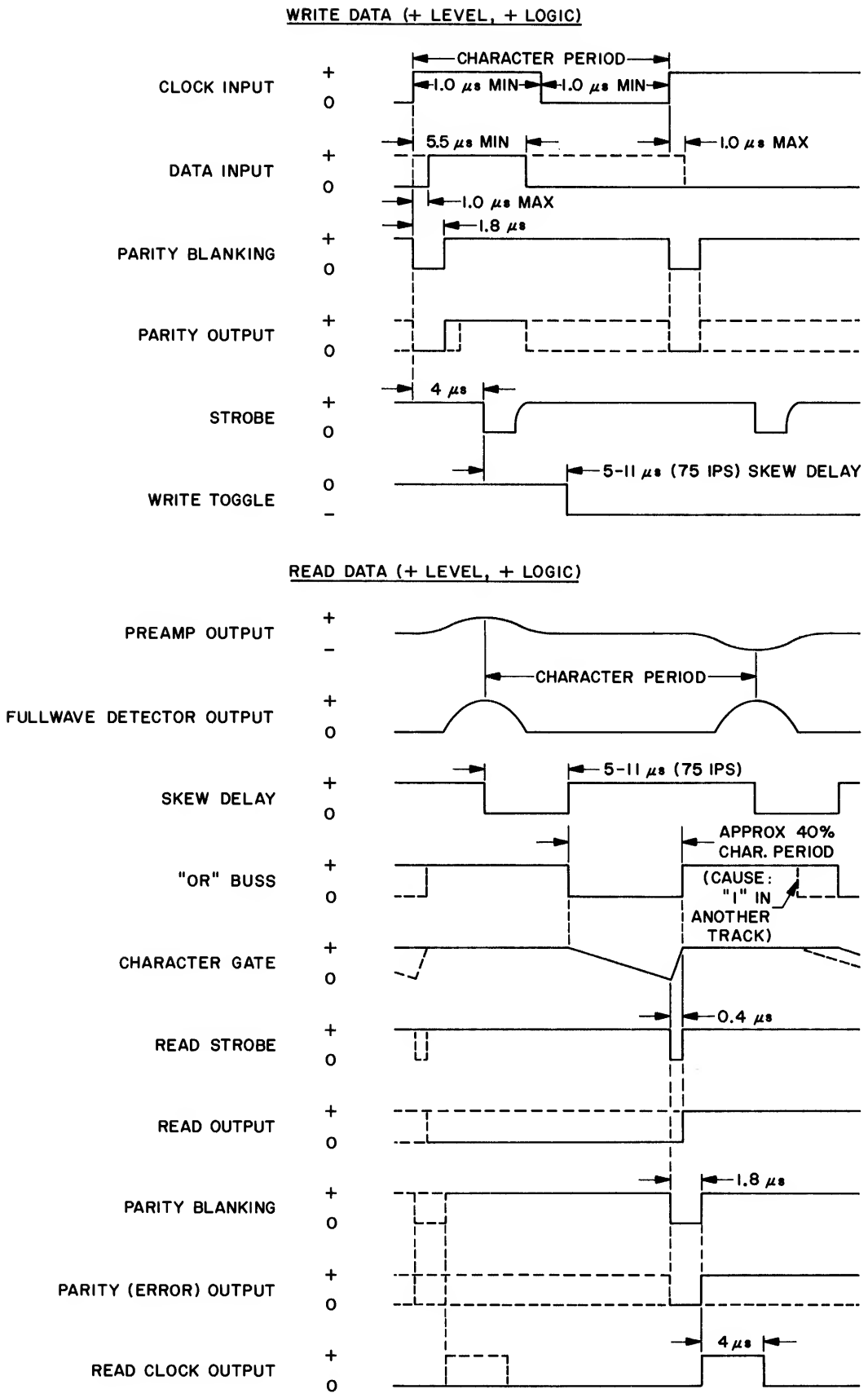


Figure 3-45. Detailed Timing Diagram for Write/Read Level System with Parity

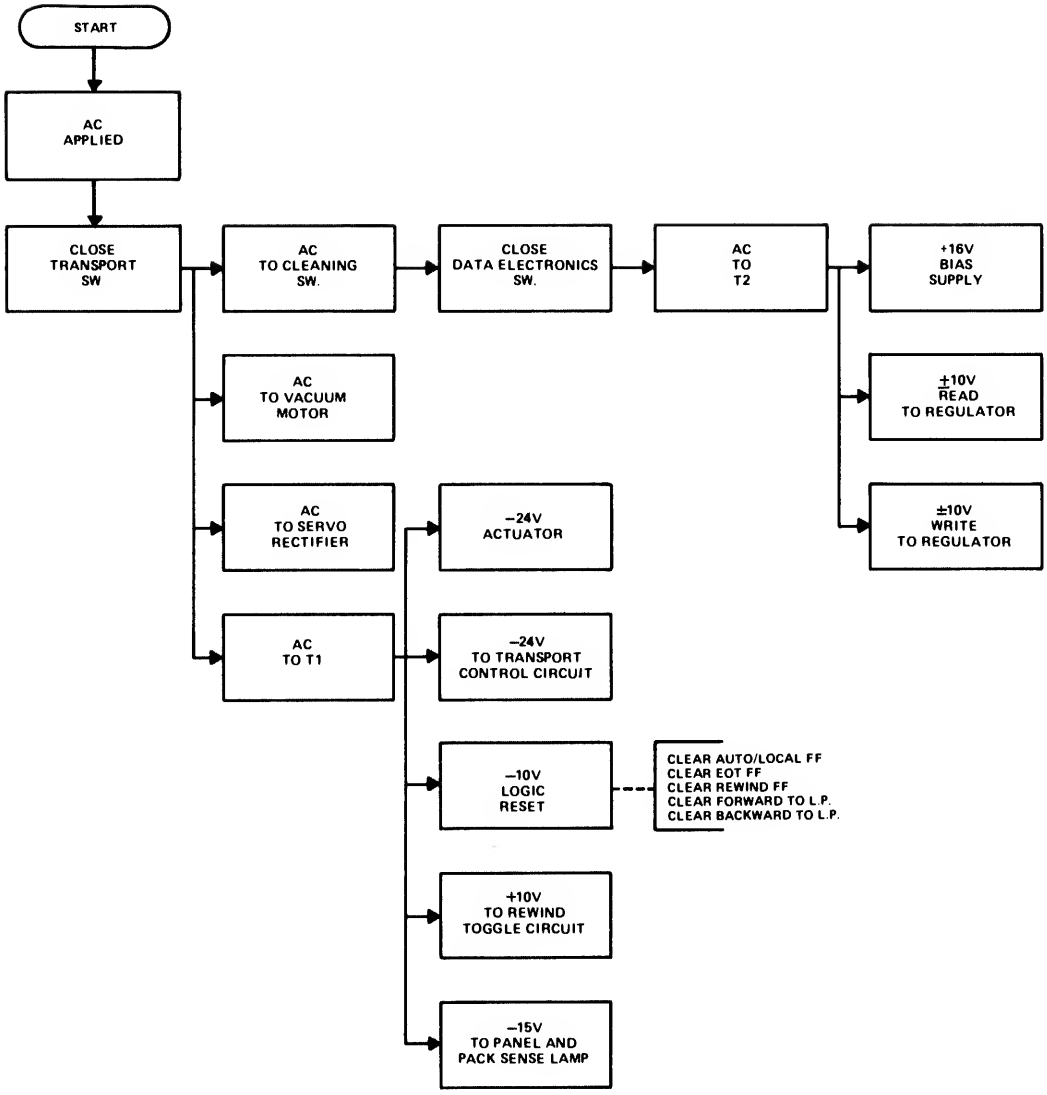


Figure 3-46. Power Up Sequence

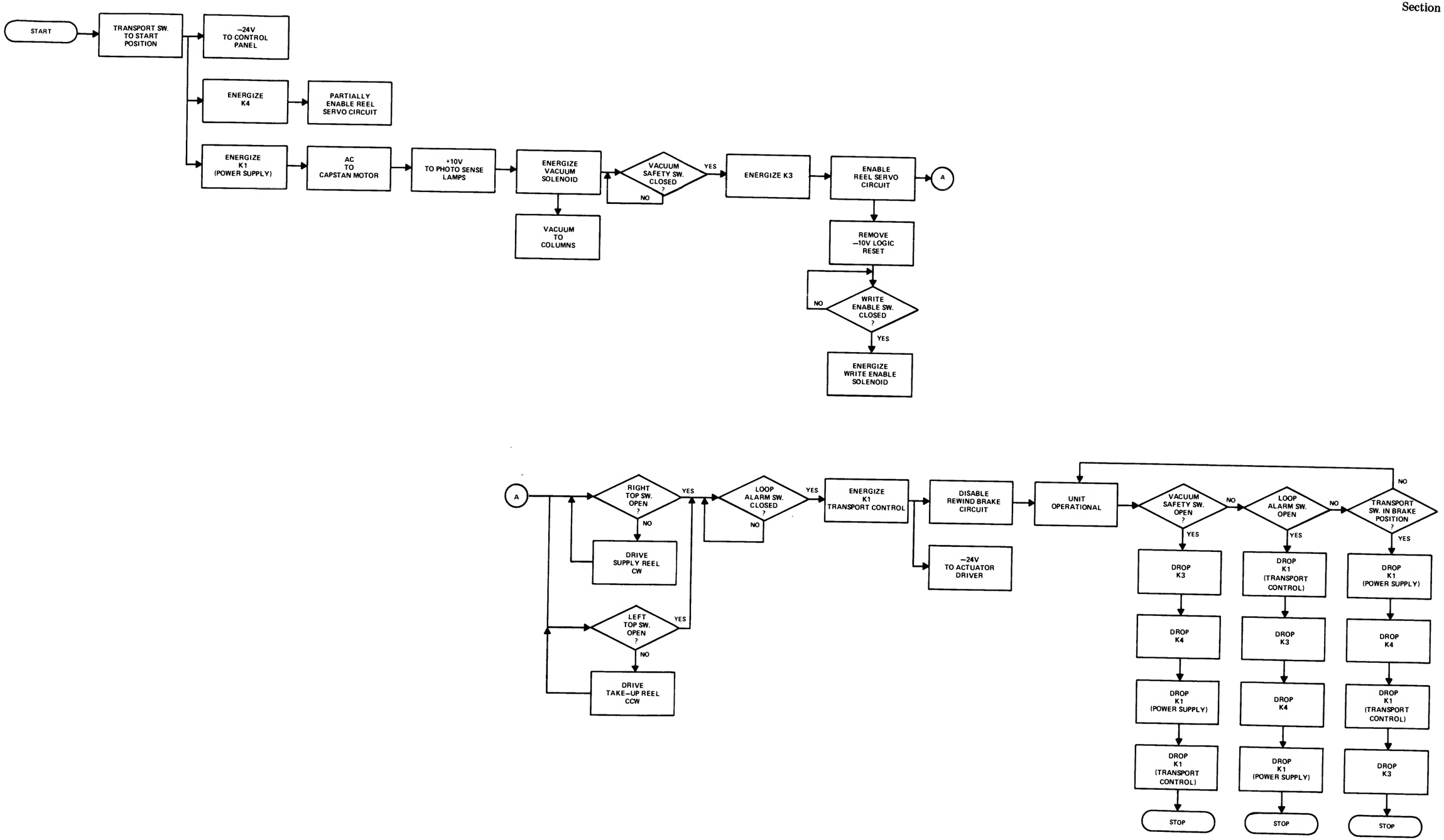


Figure 3-47. Start/Brake Sequence

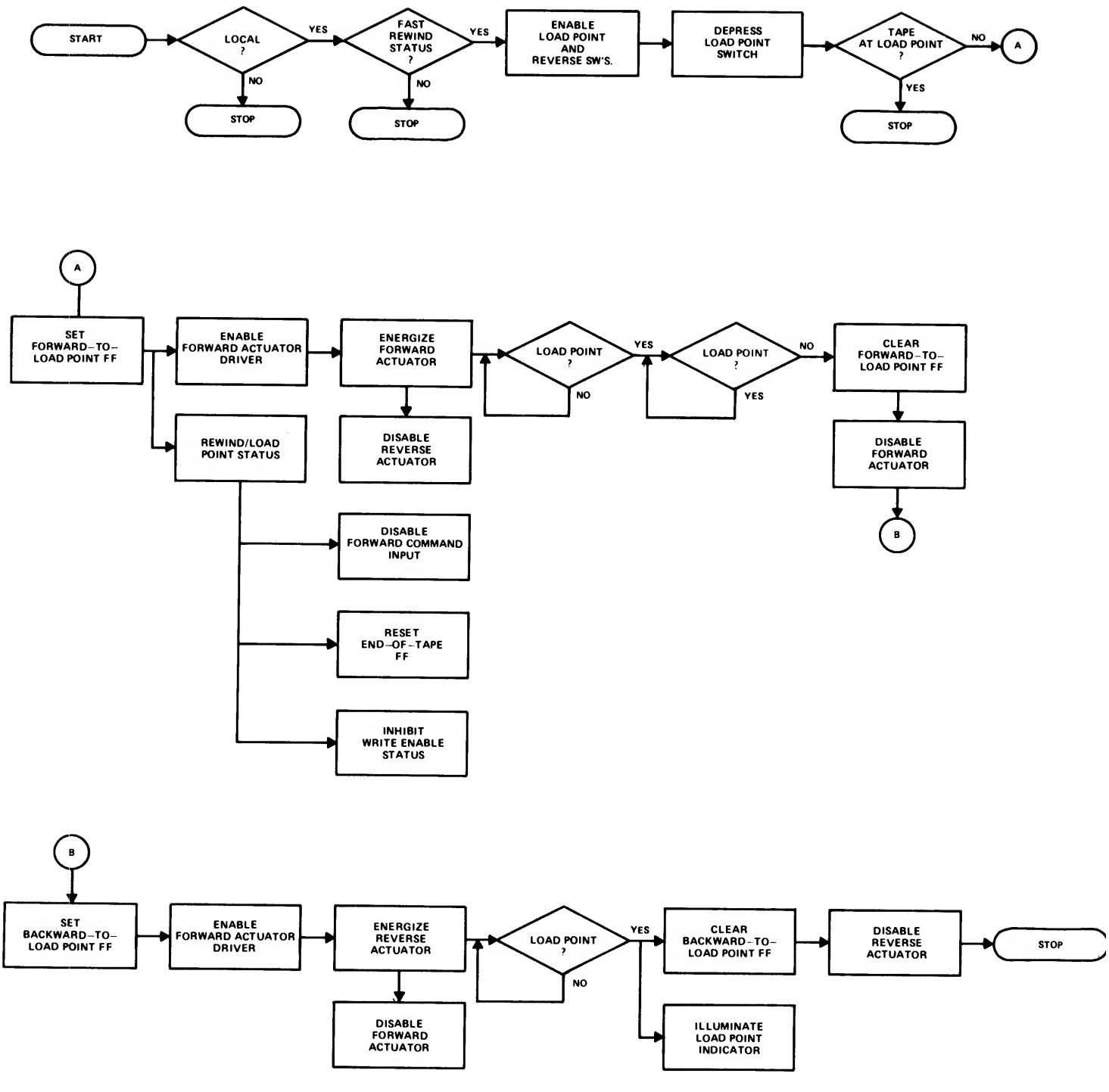


Figure 3-48. Search Load Point

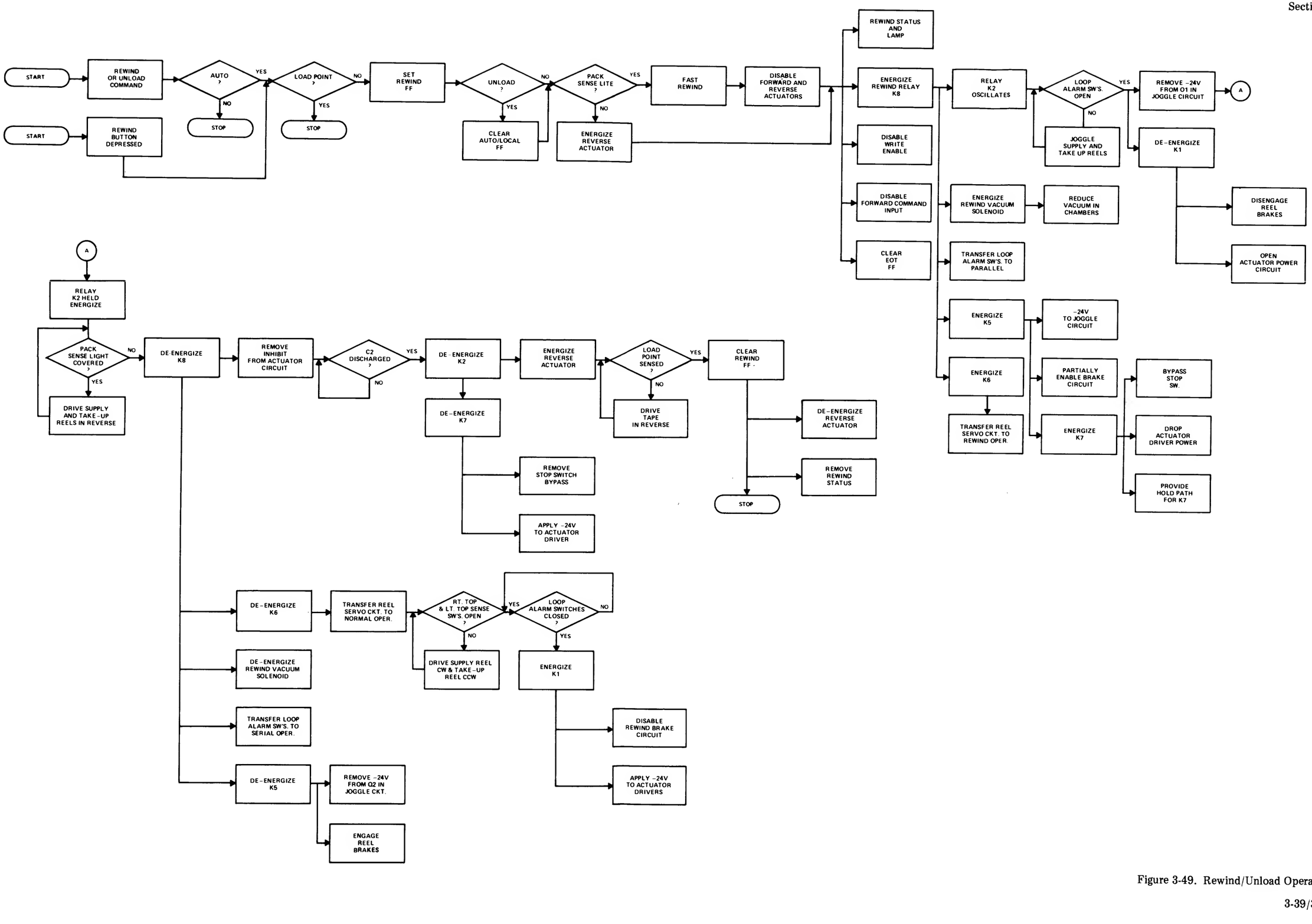
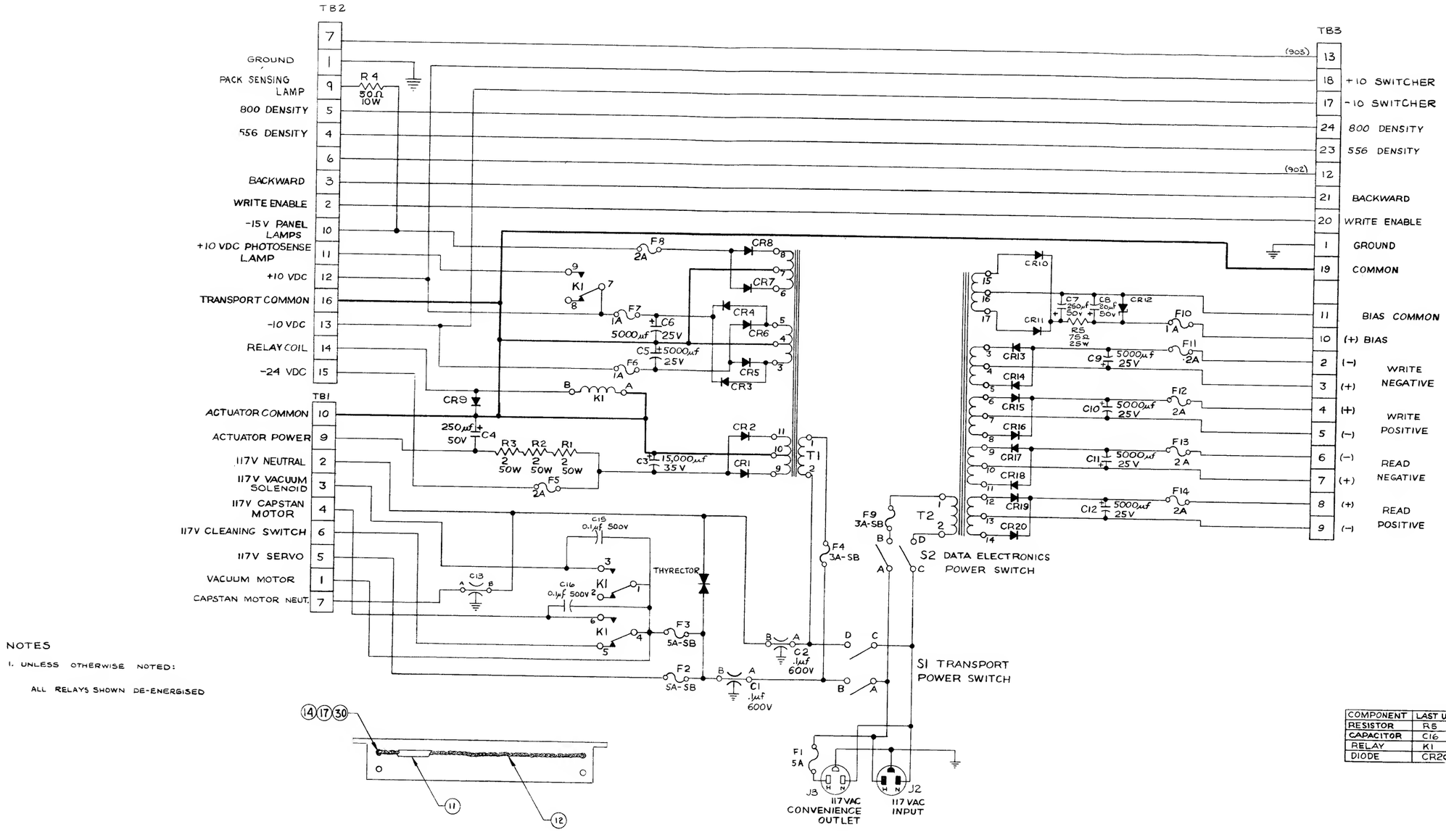


Figure 3-49. Rewind/Unload Operation

magnetic tape unit schematic diagrams

IV

SECTION IV
MAGNETIC TAPE UNIT
SCHEMATIC DIAGRAMS



NOTES

1. UNLESS OTHERWISE NOTED:

   ALL RELAYS SHOWN DE-ENERGISED

COMPONENT	LAST USED	OMITTED
RESISTOR	R5	
CAPACITOR	C16	C14
RELAY	K1	
DIODE	CR20	

POWER SUPPLY
(TRANSPORT & ELECTRONICS)
(For training purposes only)

COMPONENT	LAST USED	OMITTED
RESISTOR	R53	
CAPACITOR	C15	
TRANSISTOR	Q4	
DIODE	CR37	
SCR	SCR5	
SWITCH	S6	

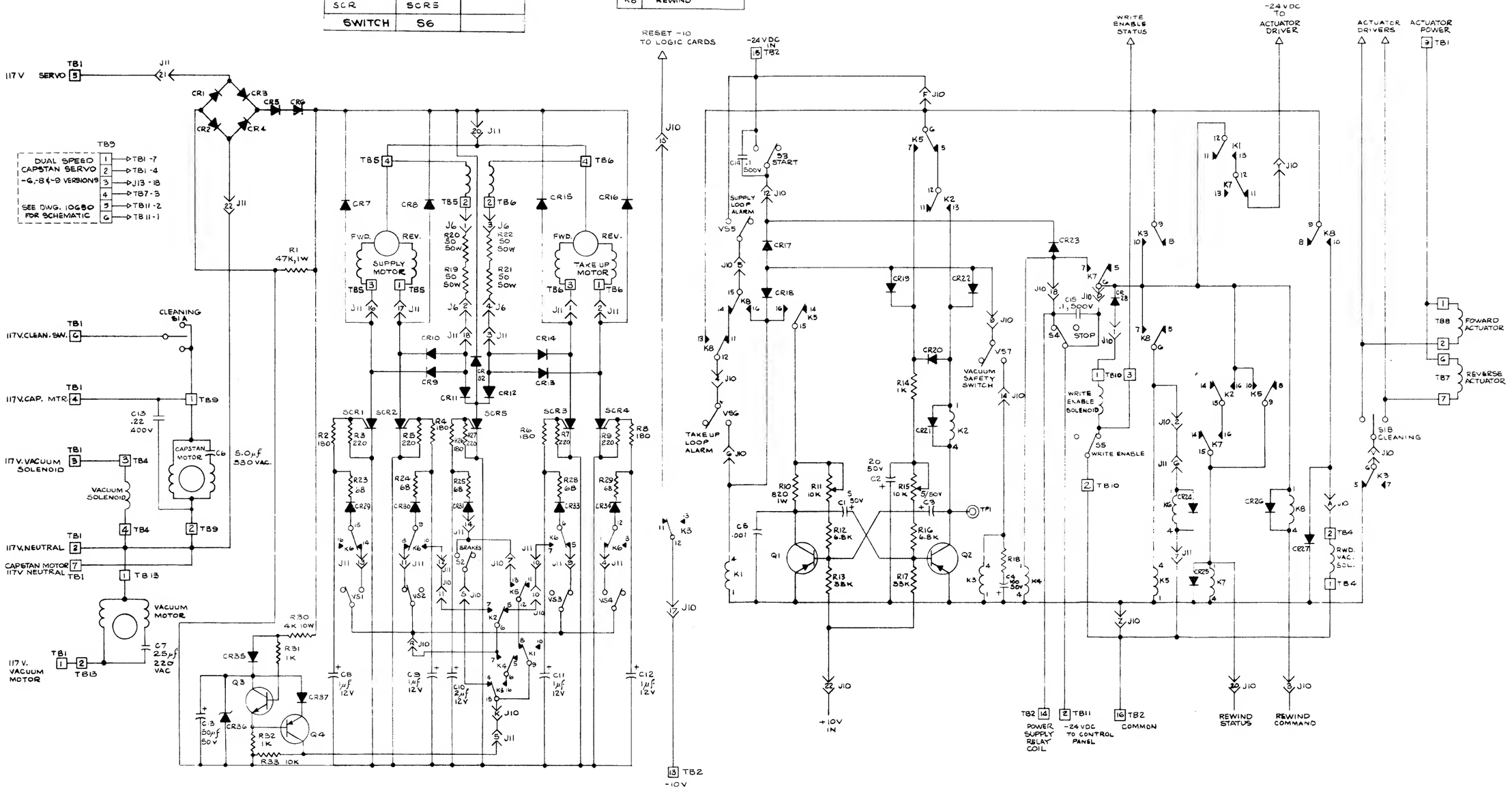
RELAY FUNCTIONS	
K1	LOOP ALARM
K2	REWIND JOGGING
K3	DISABLE
K4	REEL SERVO STOP
K5	REWIND
K6	REWIND
K7	DELAYED REWIND
K8	REWIND

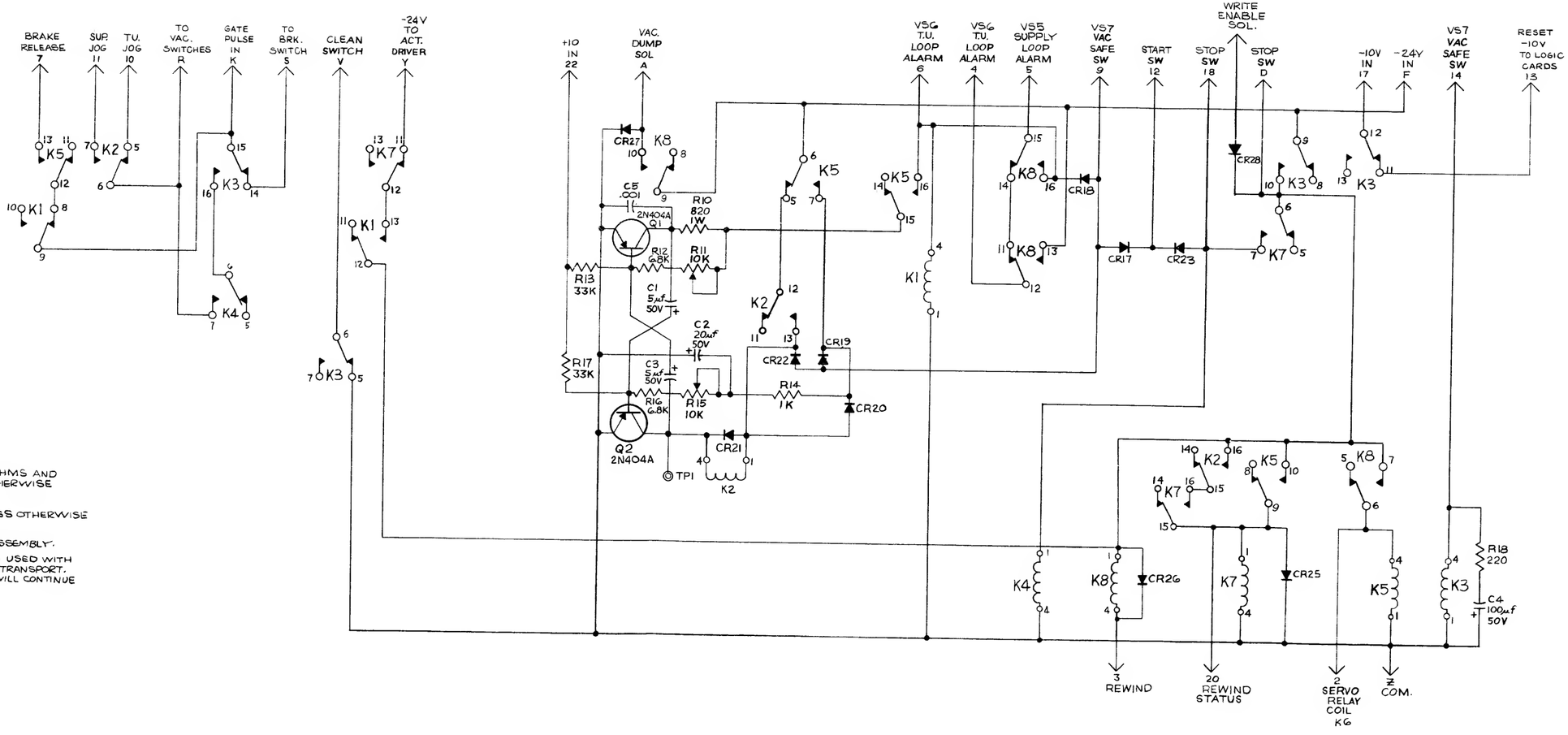
NOTE

1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTORS IN OHMS
   ALL CAPACITORS IN MICROFARADS

2. THIS SCHEMATIC APPLICABLE TO VERSIONS -0, -2 THRU -6, -8&9.

3. GROUND CONNECTION OMITTED ON SLAVE UNITS





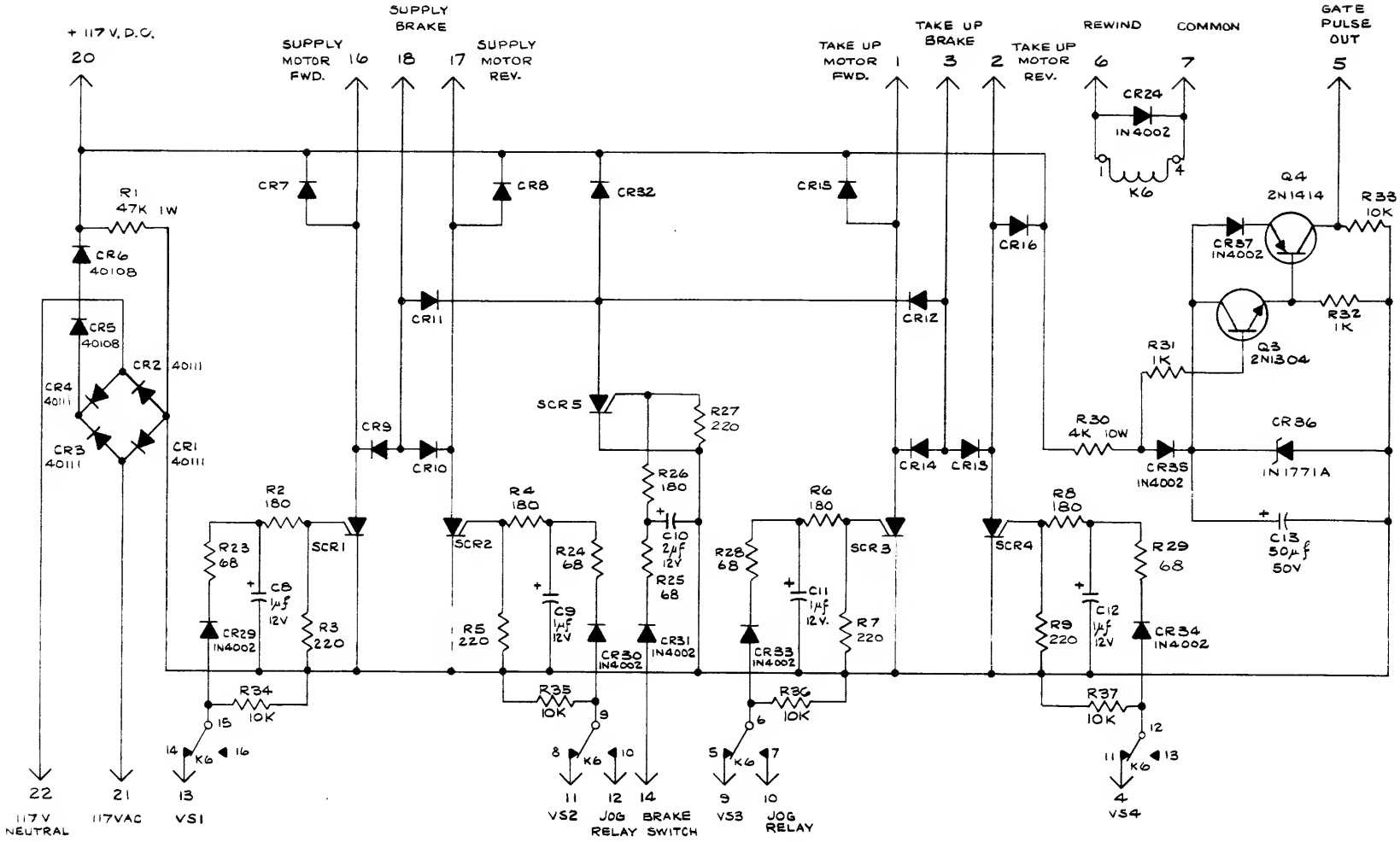
NOTES:

1. ALL RESISTOR VALUES ARE IN OHMS AND AND ARE ½ W, 5% UNLESS OTHERWISE SPECIFIED.
2. ALL DIODES ARE IN4002 UNLESS OTHERWISE SPECIFIED.
3. MARK PART NO ON SIDE "B" OF ASSEMBLY.
4. THIS CIRCUIT BOARD ASSEMBLY IS USED WITH OTHER ASSEMBLIES OF THE TAPE TRANSPORT. REFERENCE NUMBER SEQUENCE WILL CONTINUE ON THOSE ASSEMBLIES.

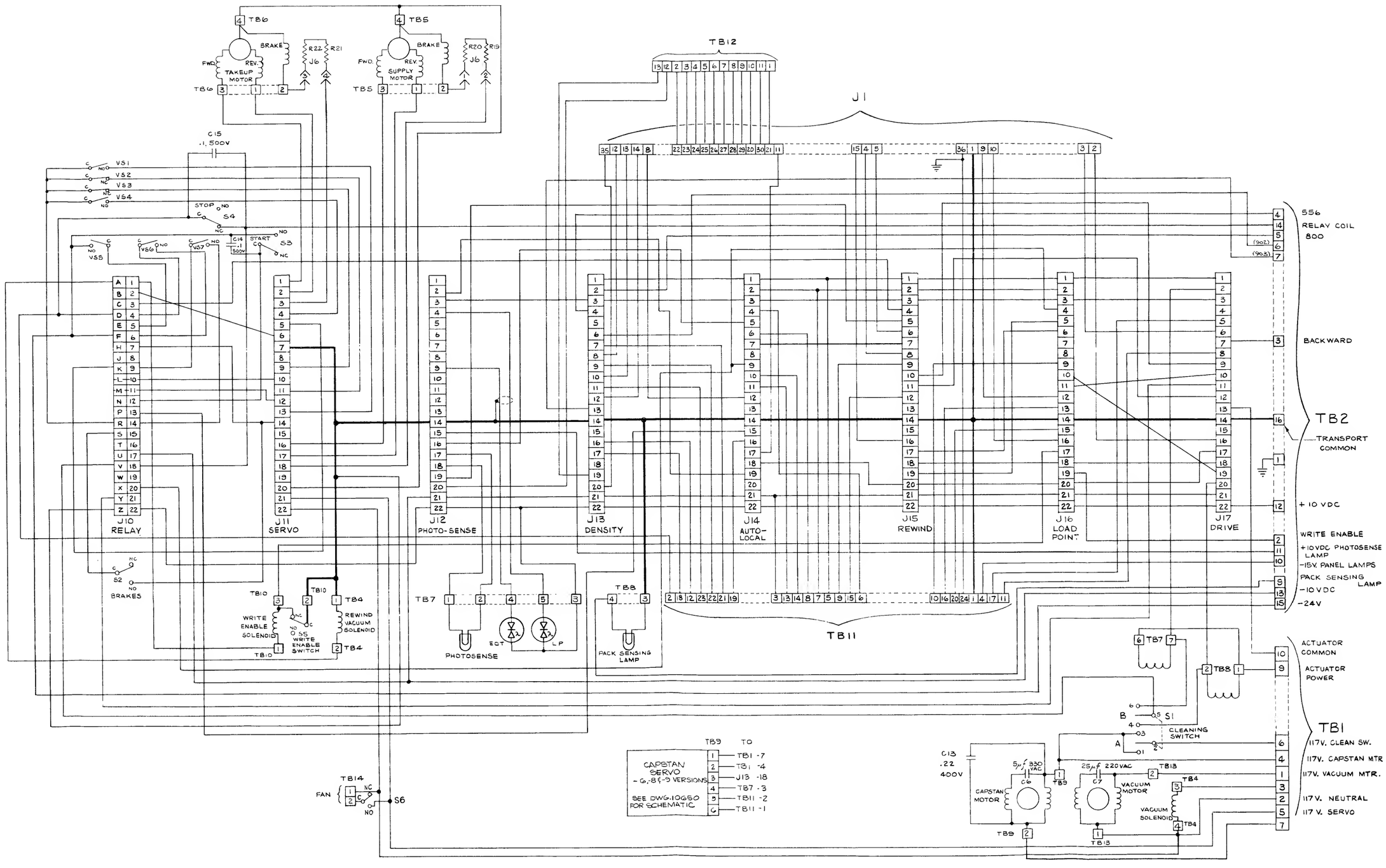
RELAY CARD
(For training purposes only)

NOTES

1. UNLESS OTHERWISE SPECIFIED ALL RESISTOR VALUES ARE RATED 1/2 W, 5%. ALL DIODES ARE TYPE IN1221
2. THIS CIRCUIT BOARD ASSEMBLY IS IS USED WITH OTHER ASSEMBLIES OF THE TAPE TRANSPORT. REFERENCE NUMBER SEQUENCE WILL CONTINUE ON THOSE ASSEMBLIES
3. MARK PART Nº ON 'B' SIDE OF ASSEMBLY

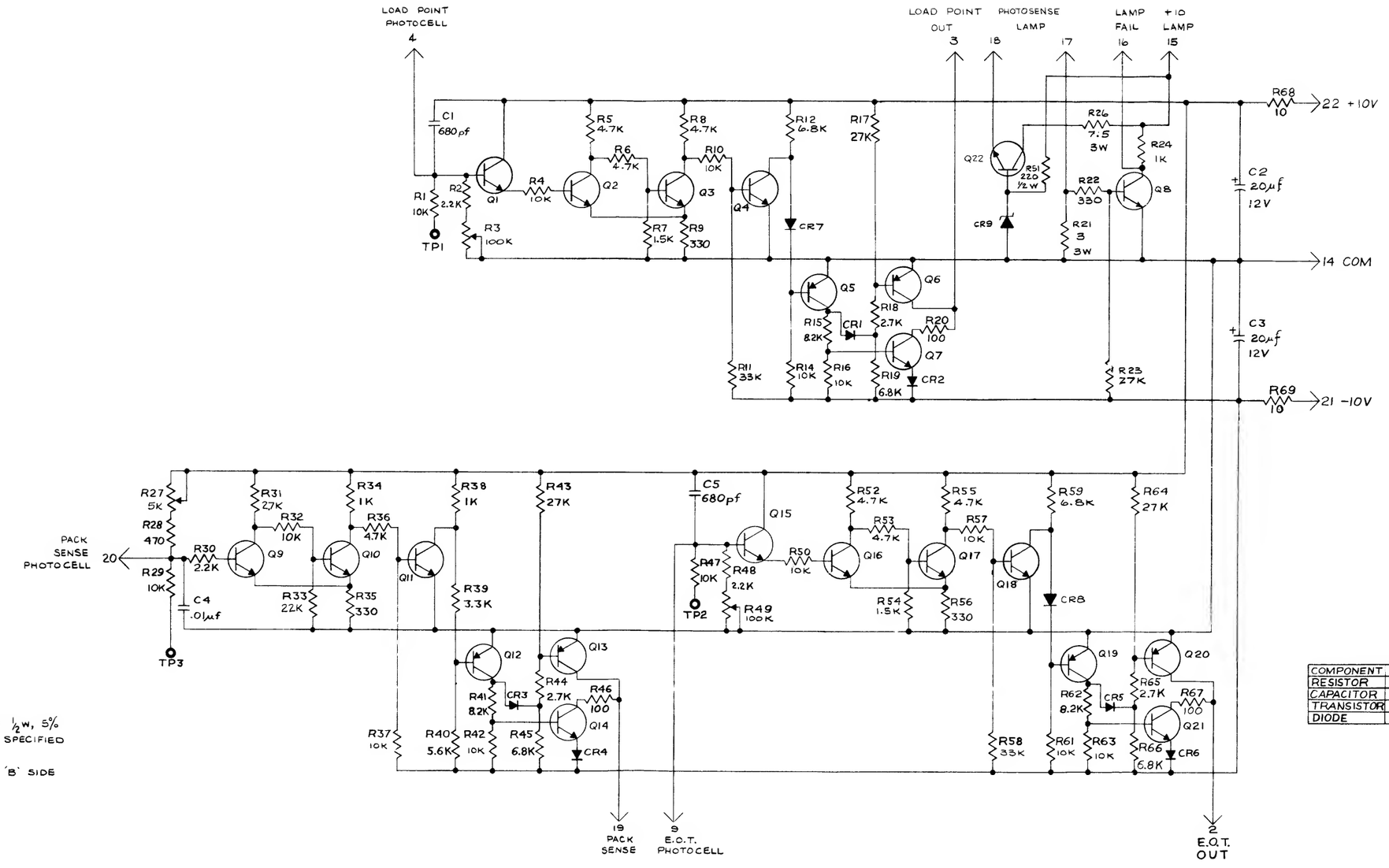


REEL SERVO CARD
(For training purposes only)



TRANSPORT WIRING
(For training purposes only)

4-11/4-12



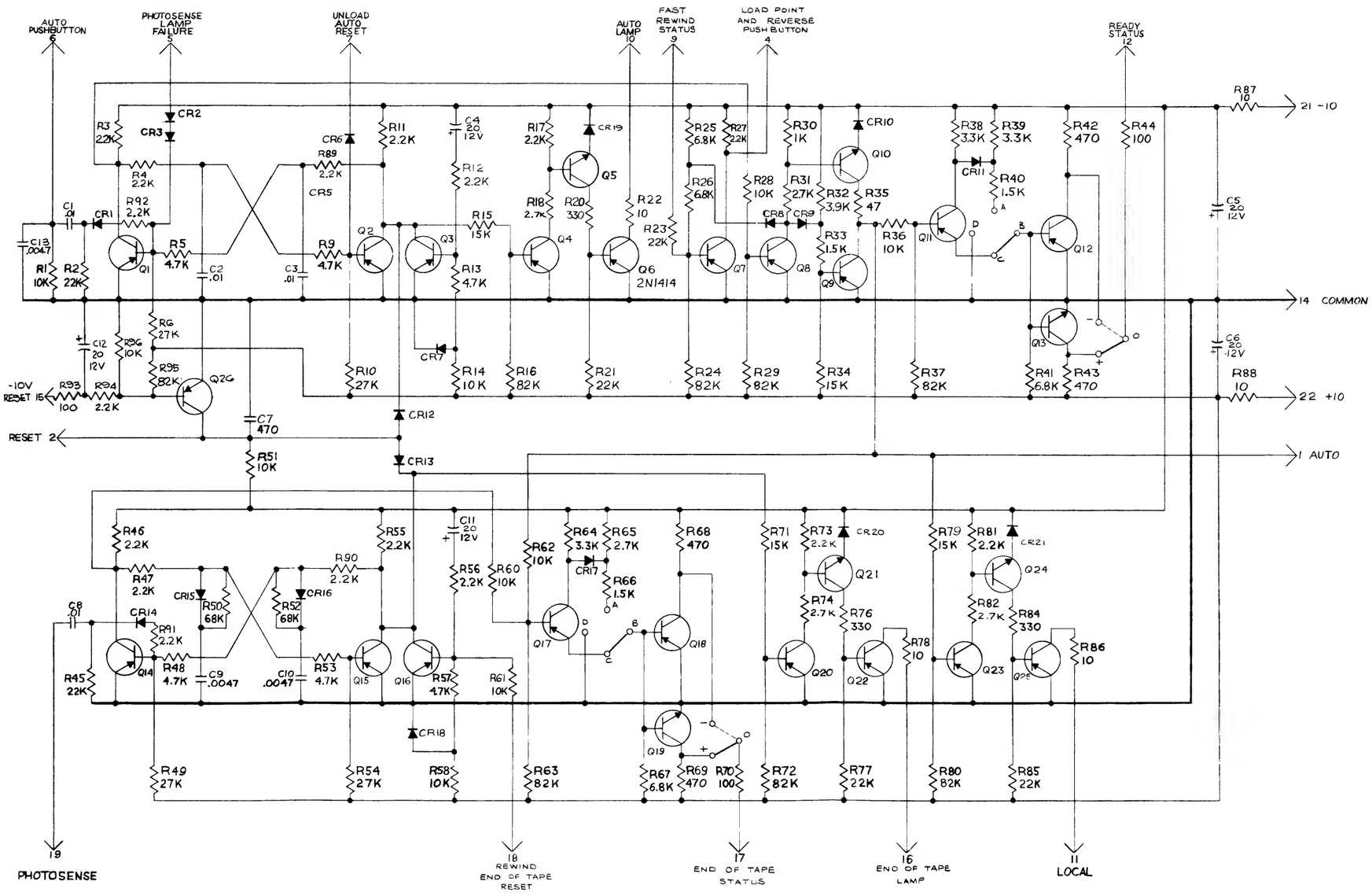
NOTE

1. ALL RESISTORS ARE ½W, 5% UNLESS OTHERWISE SPECIFIED
2. MARK PART Nº ON 'B' SIDE OF ASSEMBLY

COMPONENT	LAST USED	OMITTED
RESISTOR	R69	13,25,60
CAPACITOR	C5	
TRANSISTOR	Q22	
DIODE	CR9	

PHOTOSENSE CARD
(For training purposes only)

OUTPUT DRIVER LOGIC CONNECTIONS				
	NEGATIVE TRUE	NEGATIVE FALSE	POSITIVE TRUE	POSITIVE FALSE
JUMPER WIRES	B TO C O TO (-)	A TO B C TO D O TO (+)	A TO B C TO D O TO (+)	B TO C O TO (+)
DASHED LINES SHOWN FOR NEGATIVE TRUE OUTPUT				



NOTES

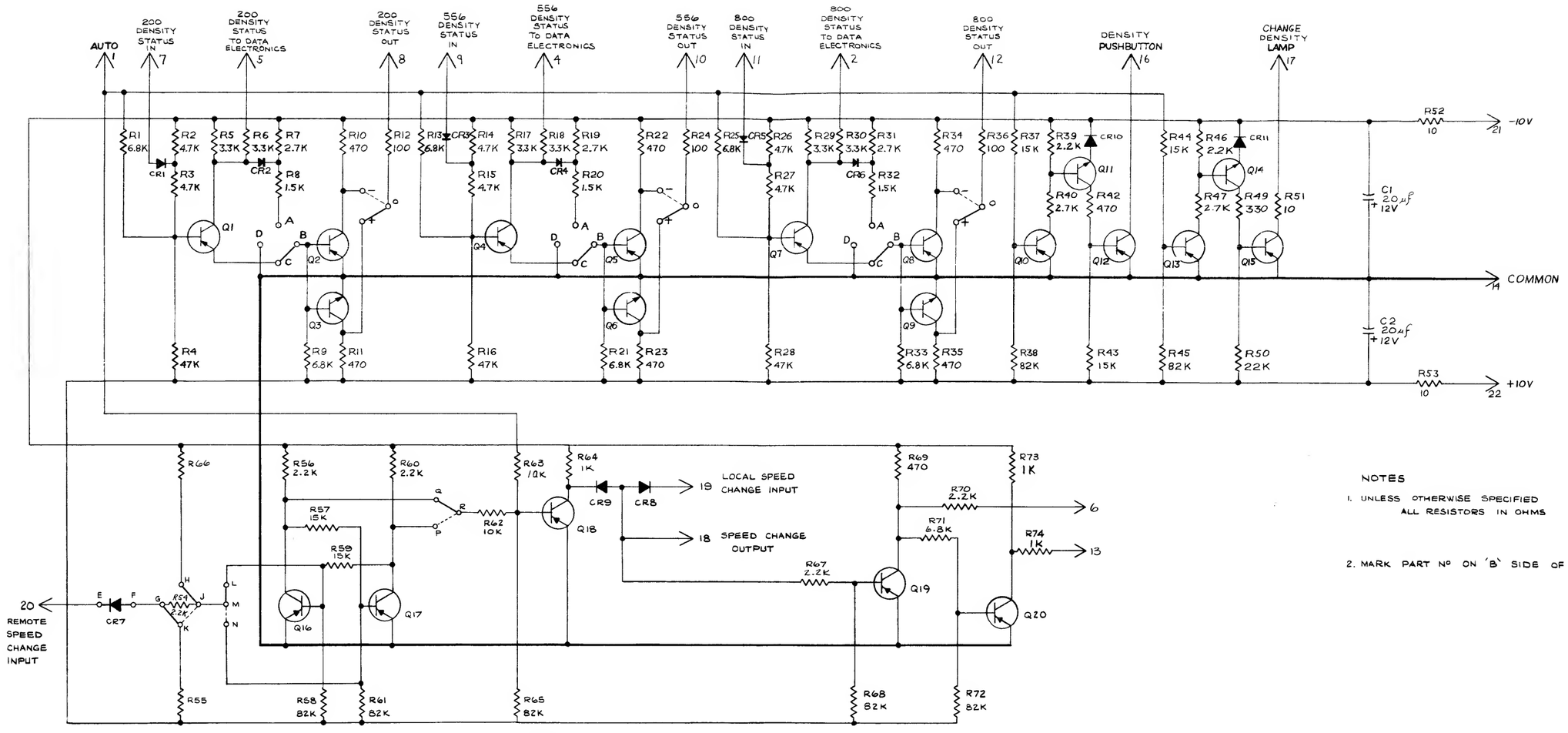
1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTORS IN OHMS

   ALL CAPACITORS IN MICROFARADS

2. MARK PART Nº ON 'B' SIDE OF ASSEMBLY

COMPONENT	LAST USED	OMITTED
RESISTOR	R96	R59,61,75,84,88
CAPACITOR	C13	
TRANSISTOR	Q26	
DIODE	CR21	CR4,5

AUTO/LOCAL & E.O.T. CARD
(For training purposes only)



NOTES

1. UNLESS OTHERWISE SPECIFIED ALL RESISTORS IN OHMS

2. MARK PART Nº ON 'B' SIDE OF ASSEMBLY

INPUT TRIGGER LOGIC CONNECTIONS					
		NEGATIVE TRUE	NEGATIVE FALSE	POSITIVE TRUE	POSITIVE FALSE
CR7	ANODE	F	E	E	F
	CATHODE	E	F	F	E
R66		NONE	4.7K	15K	15K
R55		15K	15K	NONE	4.7K
JUMPER WIRES		K TO J	G TO H	H TO J	G TO K
		M TO N	K TO J	M TO L	H TO J
		P TO R	M TO N	P TO R	M TO L
			Q TO R		Q TO R

OUTPUT DRIVER LOGIC CONNECTIONS				
	NEGATIVE TRUE	NEGATIVE FALSE	POSITIVE TRUE	POSITIVE FALSE
JUMPER WIRES	B TO C	A TO B	A TO B	B TO C
	O TO (-)	C TO D	C TO D	O TO (+)
		O TO (-)	O TO (+)	

DASHED LINES SHOWN FOR NEGATIVE TRUE OUTPUT

COMPONENT	LAST USED	OMITTED
RESISTOR	R74	R41. 48
CAPACITOR	C 2	
TRANSISTOR	Q 20	
DIODE	CR11	

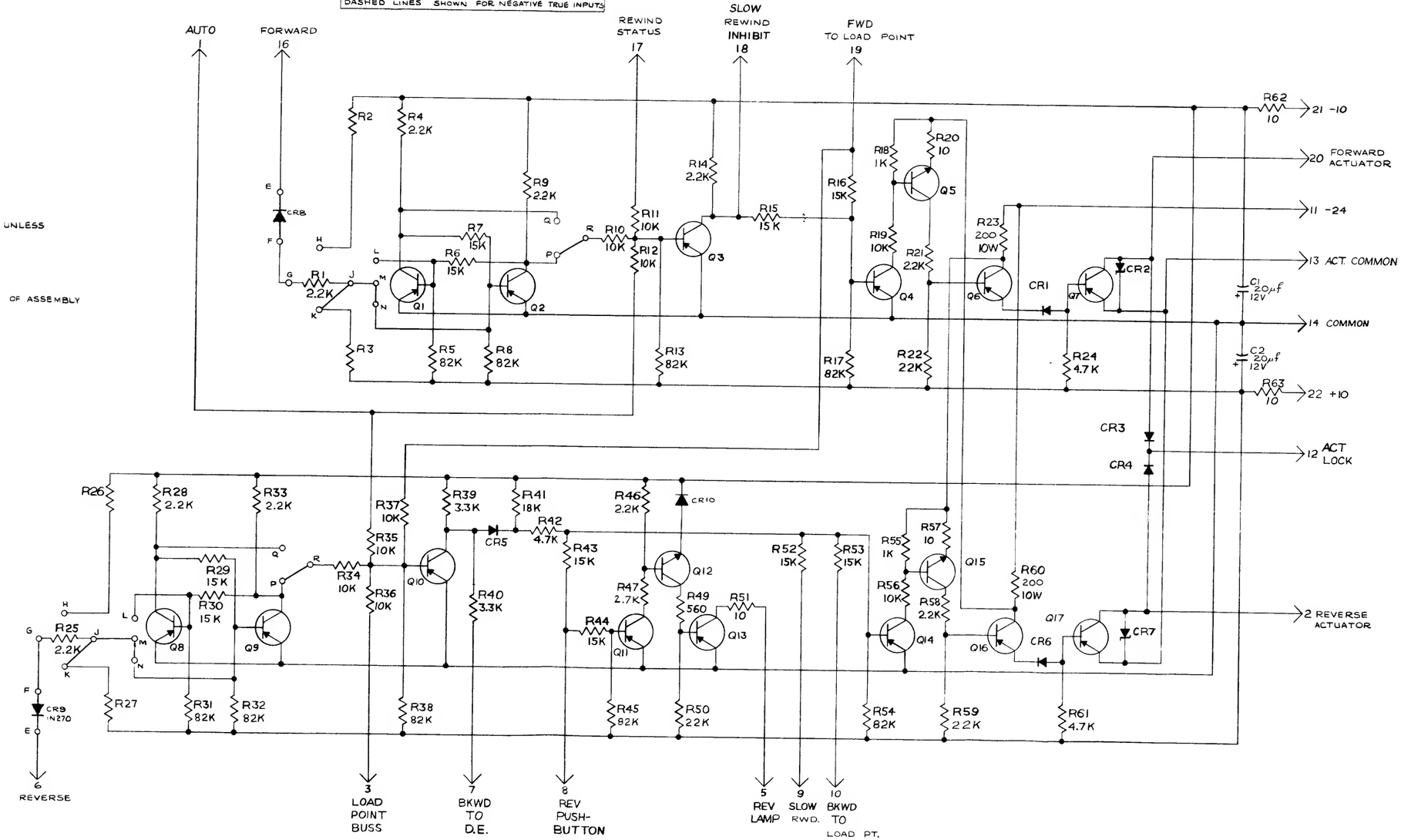
DENSITY CARD
(For training purposes only)

INPUT TRIGGER LOGIC CONNECTIONS					
		NEGATIVE TRUE	NEGATIVE FALSE	POSITIVE TRUE	POSITIVE FALSE
CR8 & CR9	ANODE	F	E	E	F
	CATHODE	E	F	F	E
R2 & R26		NONE	4.7 K	15 K	15 K
R3 & R27		15 K	15 K	NONE	4.7 K
JUMPER WIRES		K TO J	G TO H	H TO J	G TO K
		M TO N	K TO J	M TO L	H TO J
		P TO R	M TO N	P TO R	M TO L
			Q TO R		Q TO R
DASHED LINES SHOWN FOR NEGATIVE TRUE INPUTS					

COMPONENT	LAST USED	OMITTED
RESISTOR	R63	R48
CAPACITOR	C2	
TRANSISTOR	Q17	
DIODE	CR10	

NOTES

1. ALL RESISTORS 1/2W, 5% UNLESS OTHERWISE SPECIFIED
2.
3. MARK PART Nº ON 'B' SIDE OF ASSEMBLY



DRIVE CARD
(For training purposes only)

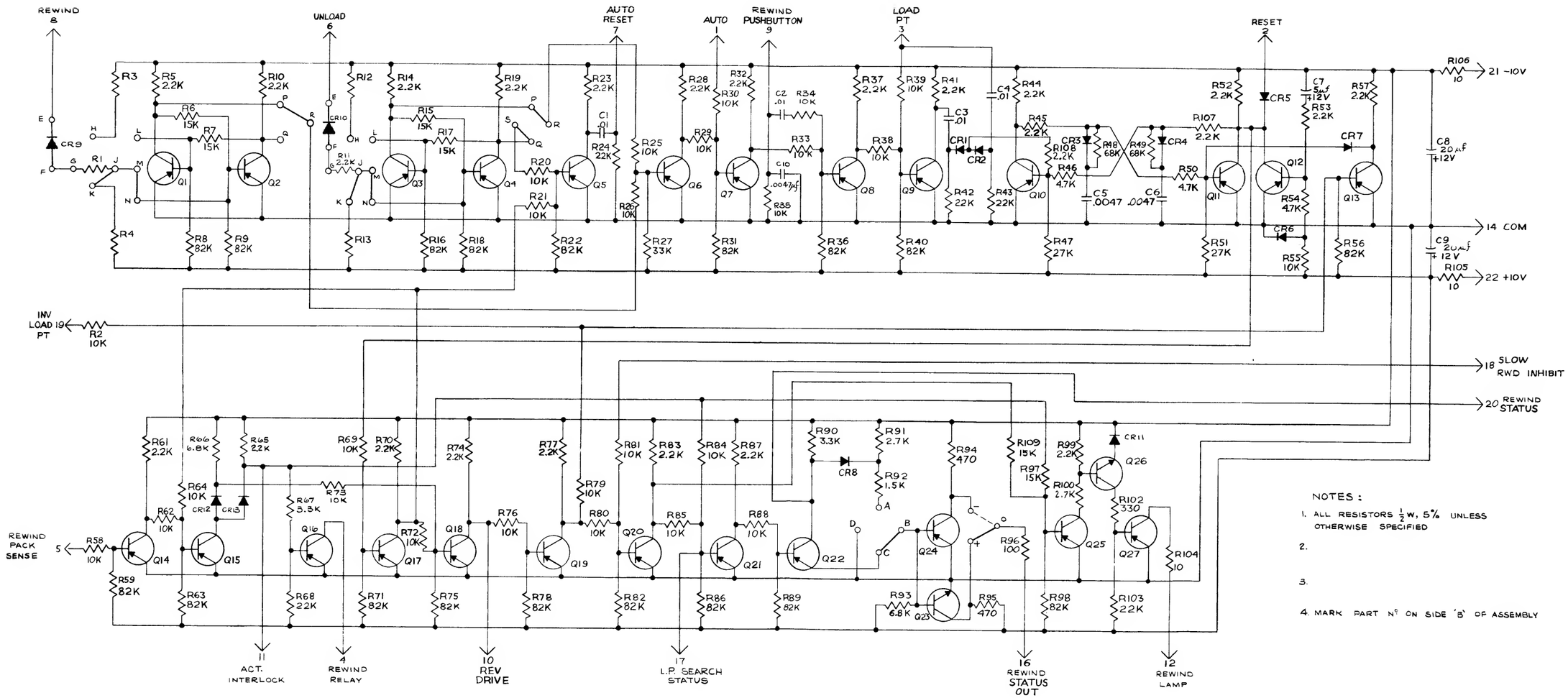
INPUT TRIGGER LOGIC CONNECTIONS					
		NEGATIVE TRUE	NEGATIVE FALSE	POSITIVE TRUE	POSITIVE FALSE
CR9 & CR10	ANODE	F	E	E	F
	CATHODE	E	F	F	E
R3 & R12		NONE	4.7 K	15K	15K
R4 & R13		15K	15K	NONE	4.7K
JUMPER WIRES		K TO J	G TO H	H TO J	G TO K
		M TO N	K TO J	M TO L	H TO J
		P TO R	M TO N	P TO R	M TO L
		S TO Q	Q TO R	S TO Q	Q TO R
			S TO P		S TO P

DASHED LINES SHOWN FOR NEGATIVE TRUE INPUTS

OUTPUT DRIVER LOGIC CONNECTIONS				
	NEGATIVE TRUE	NEGATIVE FALSE	POSITIVE TRUE	POSITIVE FALSE
JUMPER WIRES	B TO C	A TO B	A TO B	B TO C
	O TO (-)	C TO D	C TO D	C TO (+)
		O TO (-)	O TO (+)	

DASHED LINES SHOWN FOR NEGATIVE TRUE OUTPUT

COMPONENT	LAST USED	OMITTED
RESISTOR	R108	R60,101
CAPACITOR	C10	
TRANSISTOR	Q27	
DIODE	CR13	



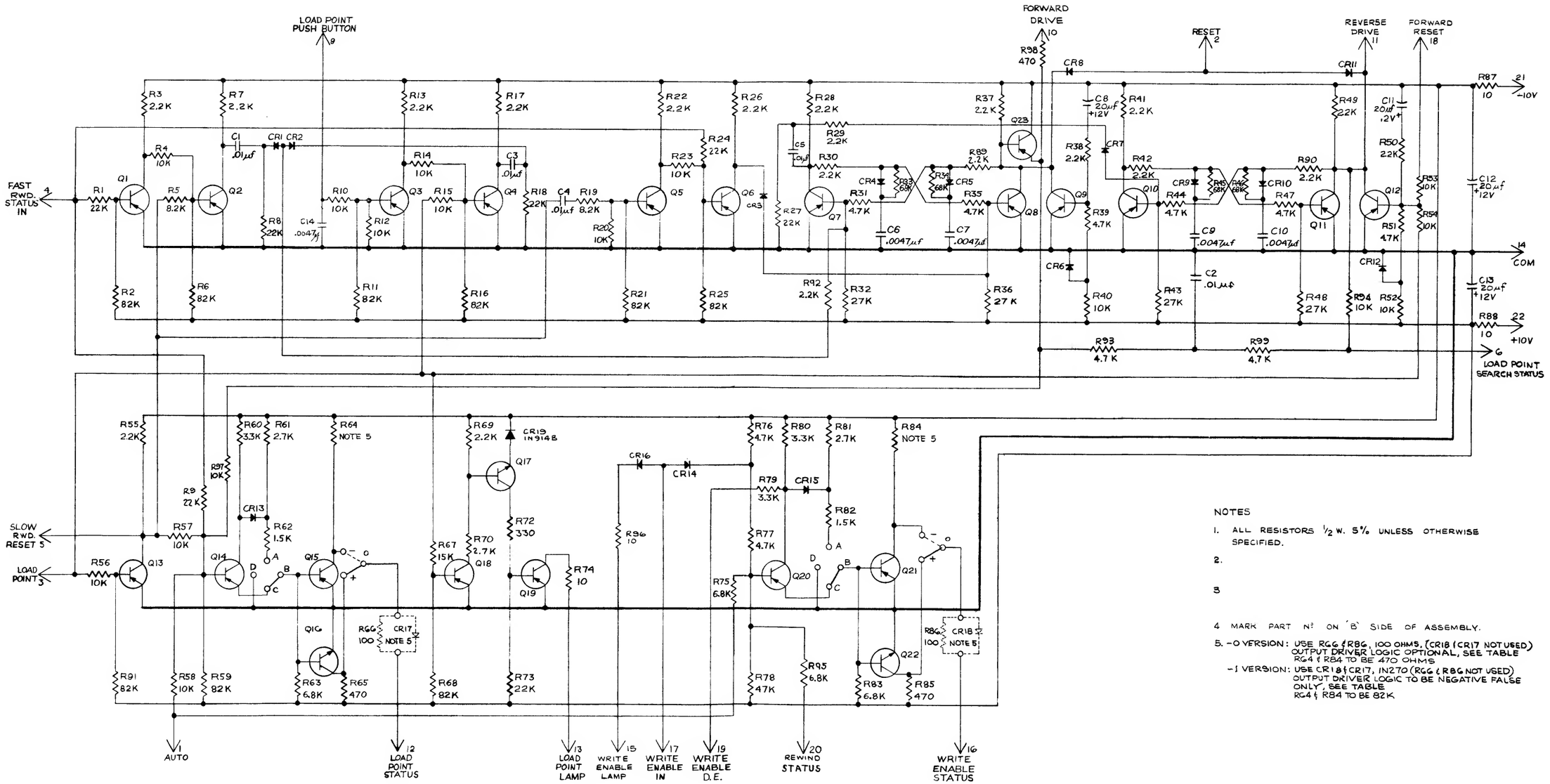
NOTES :

1. ALL RESISTORS ½ W, 5% UNLESS OTHERWISE SPECIFIED
2.
3.
4. MARK PART Nº ON SIDE 'B' OF ASSEMBLY

REWIND CARD
(For training purposes only)

COMPONENT	LAST USED	OMITTED
RESISTOR	R 99	R71
CAPACITOR	C 14	
TRANSISTOR	Q 23	
DIODE	CR 19	

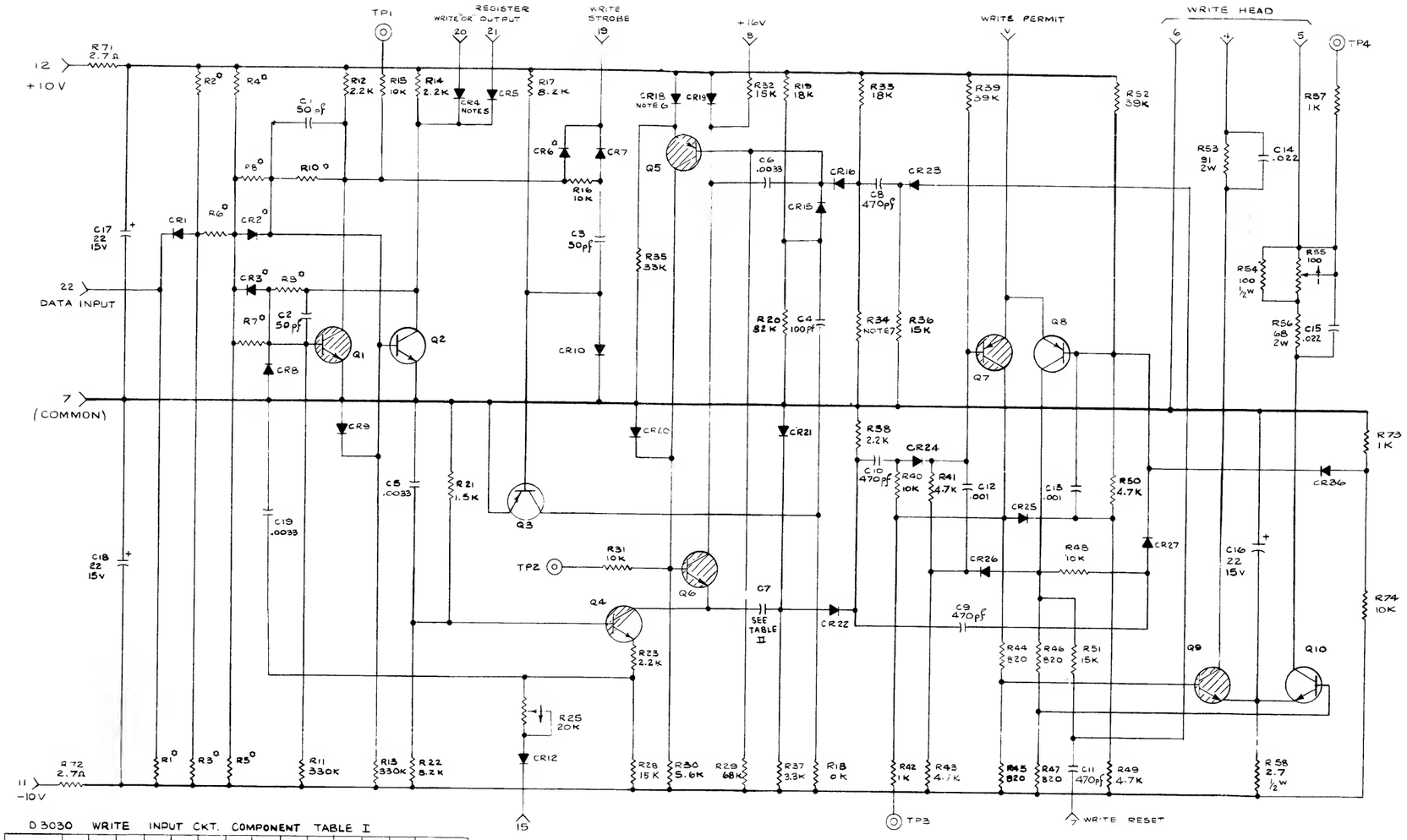
OUTPUT DRIVER LOGIC CONNECTIONS				
	NEGATIVE TRUE	NEGATIVE FALSE	POSITIVE TRUE	POSITIVE FALSE
JUMPER WIRES	B TO C	A TO B	A TO B	B TO C
	D TO (-)	C TO D	C TO D	D TO (+)
		D TO (-)	D TO (+)	
DASHED LINES SHOWN FOR NEGATIVE TRUE OUTPUT				



NOTES

1. ALL RESISTORS ½ W. 5% UNLESS OTHERWISE SPECIFIED.
2.
3.
4. MARK PART Nº ON 'B' SIDE OF ASSEMBLY.
5. -0 VERSION: USE RG6 & RB6, 100 OHMS, (CR18 (CR17 NOT USED) OUTPUT DRIVER LOGIC OPTIONAL, SEE TABLE RG4 & R84 TO BE 470 OHMS
   -1 VERSION: USE CR18 & CR17, IN270 (RG6 & RB6 NOT USED) OUTPUT DRIVER LOGIC TO BE NEGATIVE FALSE ONLY, SEE TABLE RG4 & R84 TO BE 82K

LOAD POINT & WRITE ENABLE CARD
(For training purposes only)



D 3030 WRITE INPUT CKT. COMPONENT TABLE I

		R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	CR1	CR3	CR6	CR4
PULSE	+ TRUE	27K	5.6K	—	—	10K	1.5K		—	39K	39K	IN270	—	IN270	NOTE 5 IN270
	+ FALSE	—	6.8K		—	10K	1.2K			39K	39K	—	IN270	IN270	NOTE 5 IN270
	- TRUE			8.2K	4.7K	—	1.2K		—	39K	39K		IN270	IN270	NOTE 5 IN270
	- FALSE	15K	—	8.2K	6.8K	—	1.5K	—	—	39K	39K	IN270	—	IN270	NOTE 5 IN270
LEVEL	+ TRUE	8.2K	4.7K	—	—	10K	1.5K	—	470	15K	15K	—	—	—	—
	+ FALSE	—	4.7K		—	10K	1.5K	470	—	15K	15K	—	—	—	—
	- TRUE			8.2K	6.8K	—	1.2K	470	—	15K	15K				—
	- FALSE	6.8K		8.2K	6.8K	—	1.2K	—	470	15K	15K	—	—		—

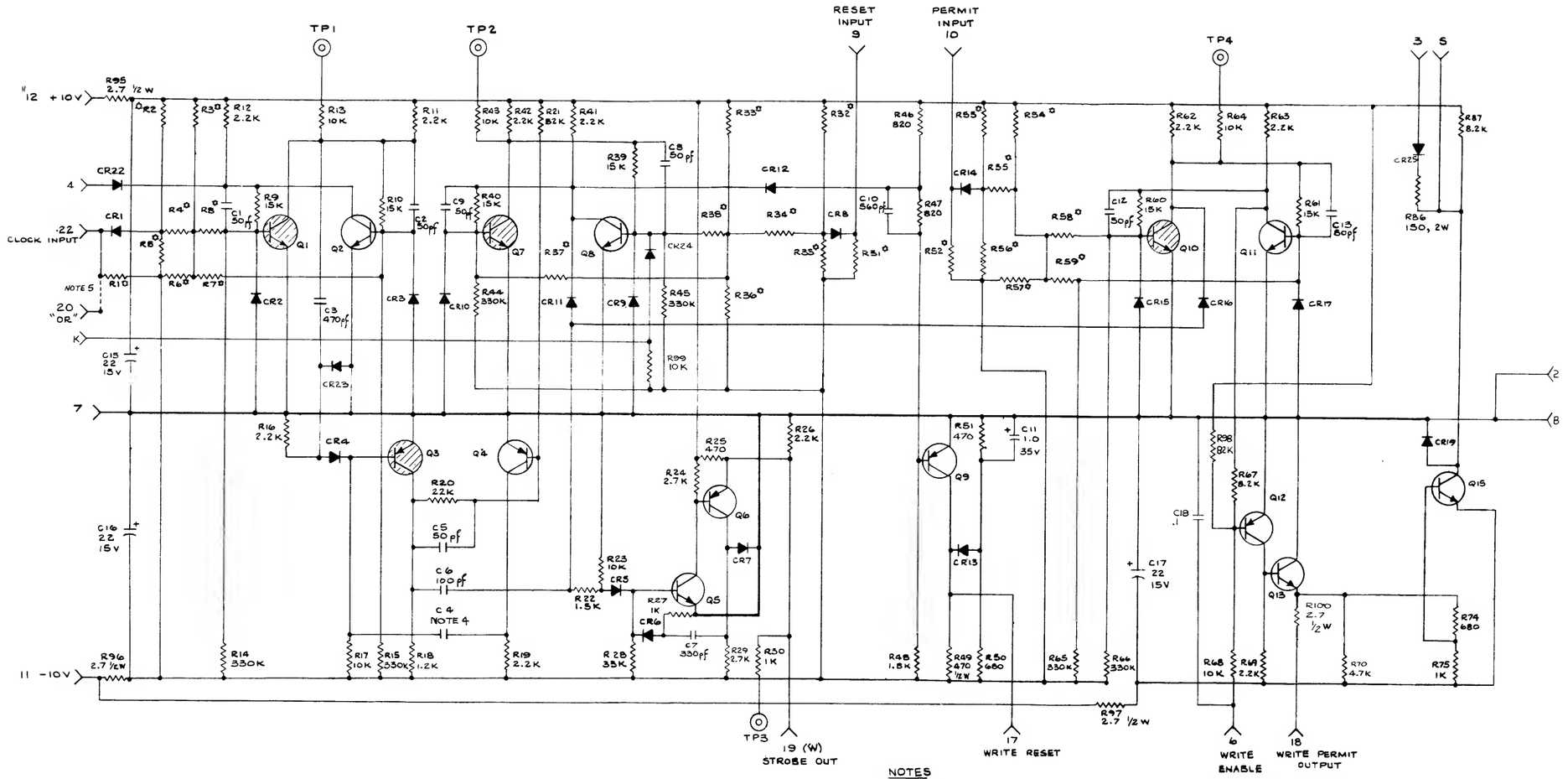
COMPONENT	LAST USED	OMITTED
RESISTOR	R74	24 26, 27, 59 THRU 70
CAPACITOR	C19	
TRANSISTOR	Q10	
DIODE	CR36	CR1, 3, 14, 17 28 - 42 38

NOTE

1. FOR COMPONENTS WITH ASTERISKS SEE COMPONENT TABLE I
2. UNLESS OTHERWISE SPECIFIED
   ALL RESISTORS IN OHMS RATED 1/2W. 5%
   ALL CAPACITORS IN MICROFARADS
3. SHEET 1 NON-SWITCHER -0, -2, -4, -6, -8 VERS. SHEET 2 SWITCHER -1, -3, -5, -7, -9 VERS.
4. SHADED TRANSISTORS ARE IN NORMAL ON STATE.
5. CR4 INSTALLED ONLY IN PULSE SYSTEMS WITHOUT SEPARATE CLOCK INPUT
6. CR18 IS REPLACED WITH A JUMPER FOR ALL VERSIONS EXCEPT -0 AND -1
7. R34 IS 82K FOR -0 AND -1 VERSIONS AND 150K 1/2 W. FOR -2 THRU -9 VERSIONS.

TABLE II

SPEED RANGE	C7	VERSION	
		NON-SWITCHER	SWITCHER
75 REF	.001	-0	-1
37.5 - 57.3	.0015	-2	-3
25.0 - 37.4	.0022	-4	-5
16.7 - 24.9	.0039	-6	-7
11.1 - 16.6	.0056	-8	-9



COMPONENT TABLE

CLOCK RESET PERMIT	R1 R31 R52	R2 R52 R53	R3 R33 R54	R4 R54 R55	R5 R55 R56	R6 R56 R57	R7 R58 R59	R8 R57 R58
+ TRUE	8.2K	4.7K	—	1.5K	—	10K	470	—
+ FALSE	—	4.7K	—	1.5K	—	10K	—	470
− TRUE	—	—	6.8K	1.2K	8.2K	—	—	470
− FALSE	6.8K	—	6.8K	1.2K	8.2K	—	470	—

COMPONENT	LAST USED	OMITTED
RESISTOR	R100	71, 72, 73, 76 THRU 85, 88 THRU 92
CAPACITOR	C18	C14
DIODE	CR26	CR18,20,21,26
TRANSISTOR	Q15	Q14, 16, 17, 18 19, 20, 21

NOTES

1. FOR COMPONENTS WITH ASTERISKS SEE COMPONENT TABLE
2. UNLESS OTHERWISE SPECIFIED

   ALL RESISTORS IN OHMS RATED 1/4 W. 5%
   ALL CAPACITORS IN MICROFARADS

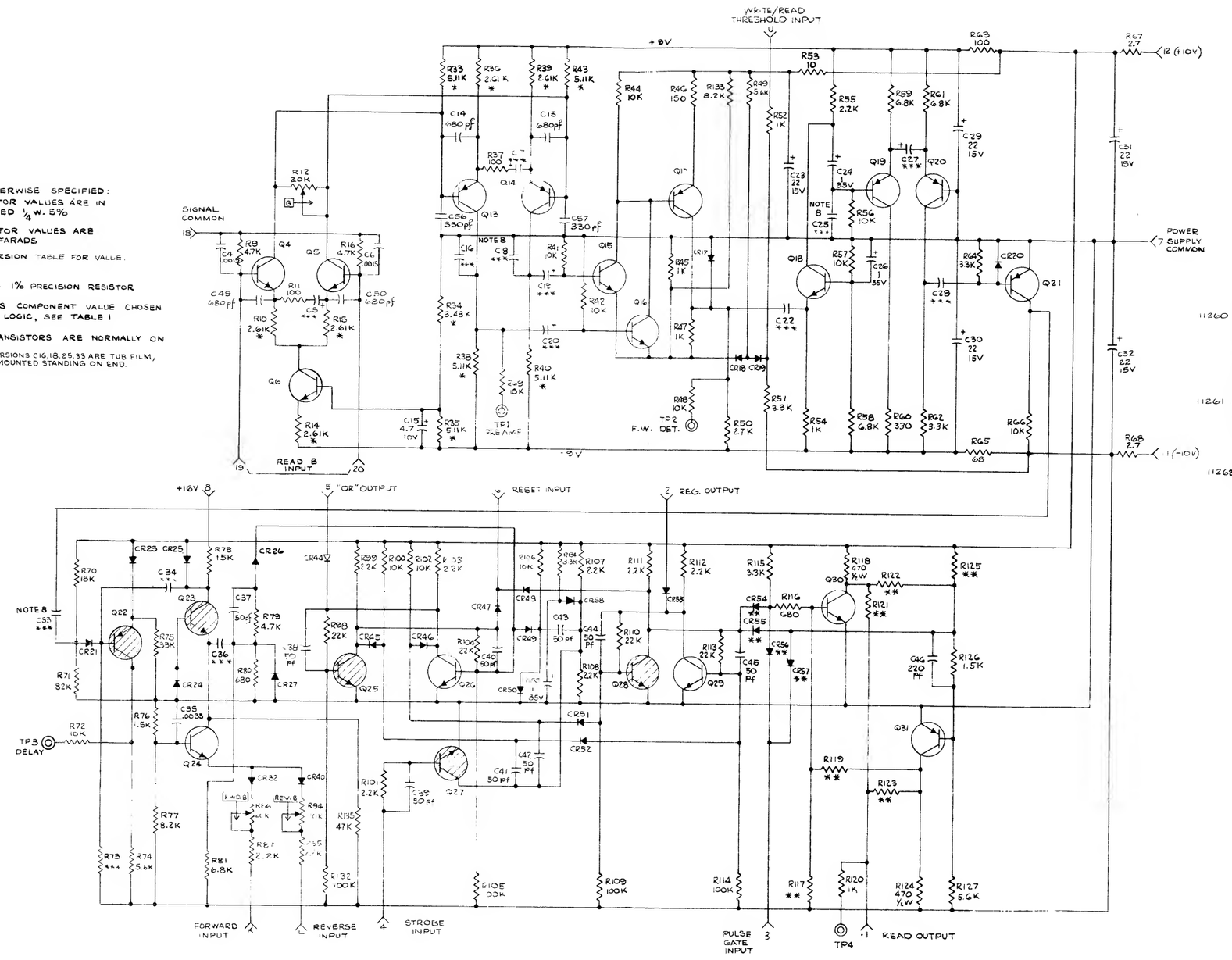
3. SHADED TRANSISTORS ARE IN NORMAL ON STATE
4. FOR LEVEL SYSTEMS C4 TO BE 470 pf. FOR PULSE SYSTEMS C4 TO BE 680 pf.
5. STRAP FOR "OR" INPUT INSTALLED ONLY IN PULSE SYSTEMS WITHOUT SEPARATE CLOCK INPUT. FOR SUCH SYSTEMS, STRAP WRITE CLOCK INPUT FOR POSITIVE FALSE LOGIC

TABLE I

LOGIC	R117	R119	R121	R122	R123	R125	CR54	CR55	CR56	CR57
						(PULSE SYSTEMS ONLY)				
+TRUE	-	1.5K	100	—		3.3K	—	IN270	—	IN270
+FALSE	10K	—	100	—	—	—	IN270	—	IN270	—
-TRUE	—	—	—	—	100	3.3K	—	IN270	—	IN270
-FALSE	10K	—	—	100	100	—	IN270	—	IN270	—

NOTES

1. UNLESS OTHERWISE SPECIFIED: ALL RESISTOR VALUES ARE IN OHMS RATED 1/4 W. 5%
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. *** SEE VERSION TABLE FOR VALUE.
4.
5. * INDICATES 1% PRECISION RESISTOR
6. ** INDICATES COMPONENT VALUE CHOSEN FOR OUTPUT LOGIC, SEE TABLE I
7. SHADED TRANSISTORS ARE NORMALLY ON
8. ON CERTAIN VERSIONS C16,18,25,33 ARE TUB FILM, AND MUST BE MOUNTED STANDING ON END.



VERSION TABLE NON-SWITCHER

	SPD. I.P.S.	C5	C36	C34	C33	R73	C25	C22	C28	C16 C18	C19 C20	C17 C27	VER
11260	REF. 75	22	.001	.0033	100pf	68K	470pf	.001	.0033	680pf	1	4.7	-0
	37.5 TO 57.5	22	.0015	.0035	100pf	68K	470pf	.0022	.0033	680pf	1	10	-4
	25.0 TO 37.4	22	.0022	.0033	100pf	68K	.001	.0022	.0082	.0018	1	10	-6
	14.7 TO 24.9	22	.0039	JUMP	470pf	47K	.001	.0039	.012	.0027	1	10	-8
11261	11.1 TO 16.6	22	.0056	JUMP	470pf	33K	.0022	.0056	.018	.0039	1	10	-0
	7.42 TO 11.0	22	.0082	JUMP	.001	33K	.0039	.0082	.027	.0056	2.2	22	-2
	4.95 TO 7.41	22	.015	JUMP	.001	33K	.0082	.015	.039	.0082	2.2	22	-4
	3.29 TO 4.94	22	.018	JUMP	.001	33K	.0082	.018	.056	.012	2.2	22	-6
	2.19 TO 3.28	47	.027	JUMP	.001	33K	.012	.027	.15	.022	4.7	47	-8
11262	1.46 TO 2.18	47	.047	JUMP	.001	33K	.022	.047	.15	.027	4.7	47	-0
	1.00 TO 1.45	100	.068	JUMP	.001	33K	.033	.068	.22	.039	10	100	-2

NOTE: CR23 IS REPLACED WITH A JUMPER, AND R75 IS NOT USED FOR ANY SPEED BELOW 75 I.P.S.

COMPONENT	LAST USED	OMITTED
RESISTOR	R135	1 THRU 8, 17 THRU 32, 82 THRU 85 88 THRU 93 96, 97, 128 THRU 131
CAPACITOR	C57	C1, 2, 3 7 THRU 12,21
TRANSISTOR	Q31	Q1, 2, 3, 7 THRU 12
DIODE	CR58	CR1 THRU 16,22 28 THRU 31 33 THRU 39 41, 42, 43

READ CARD
(For training purposes only)

NOTES

1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTORS IN OHMS, 1/4 W.
   ALL CAPACITORS IN MICROFARADS

2. SHADED TRANSISTORS ARE NORMALLY ON

3 FOR COMPONENTS WITH ASTERISKS SEE COMPONENT TABLE.

COMPONENT	LAST USED	OMITTED
RESISTOR	R140	R1 THRU 43, 47, 48, 67
CAPACITOR	C32	C1 THRU 10, 5
TRANSISTOR	Q33	Q1 THRU 12
DIODE	CR40	CR1 THRU 11, 13, 37

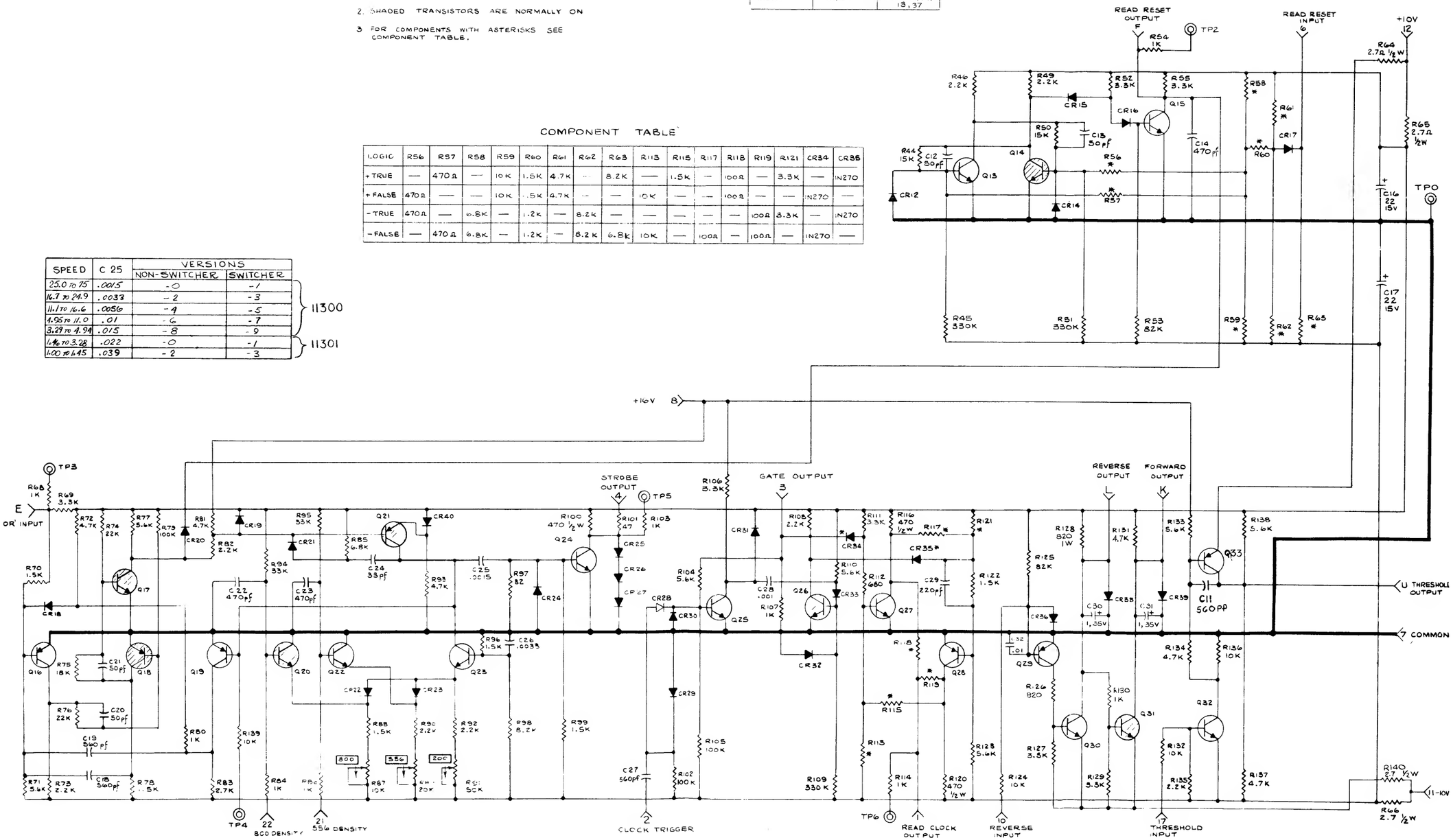
COMPONENT TABLE

LOGIC	R56	R57	R58	R59	R60	R61	R62	R63	R113	R115	R117	R118	R119	R121	CR34	CR35
+TRUE	—	470Ω	—	10K	1.5K	4.7K	—	8.2K	—	1.5K	—	100Ω	—	3.3K	—	IN270
+FALSE	470Ω	—	—	10K	1.5K	4.7K	—	—	10K	—	—	100Ω	—	—	IN270	—
-TRUE	470Ω	—	6.8K	—	1.2K	—	8.2K	—	—	—	—	—	100Ω	3.3K	—	IN270
-FALSE	—	470Ω	6.8K	—	1.2K	—	8.2K	6.8K	10K	—	100Ω	—	100Ω	—	IN270	—

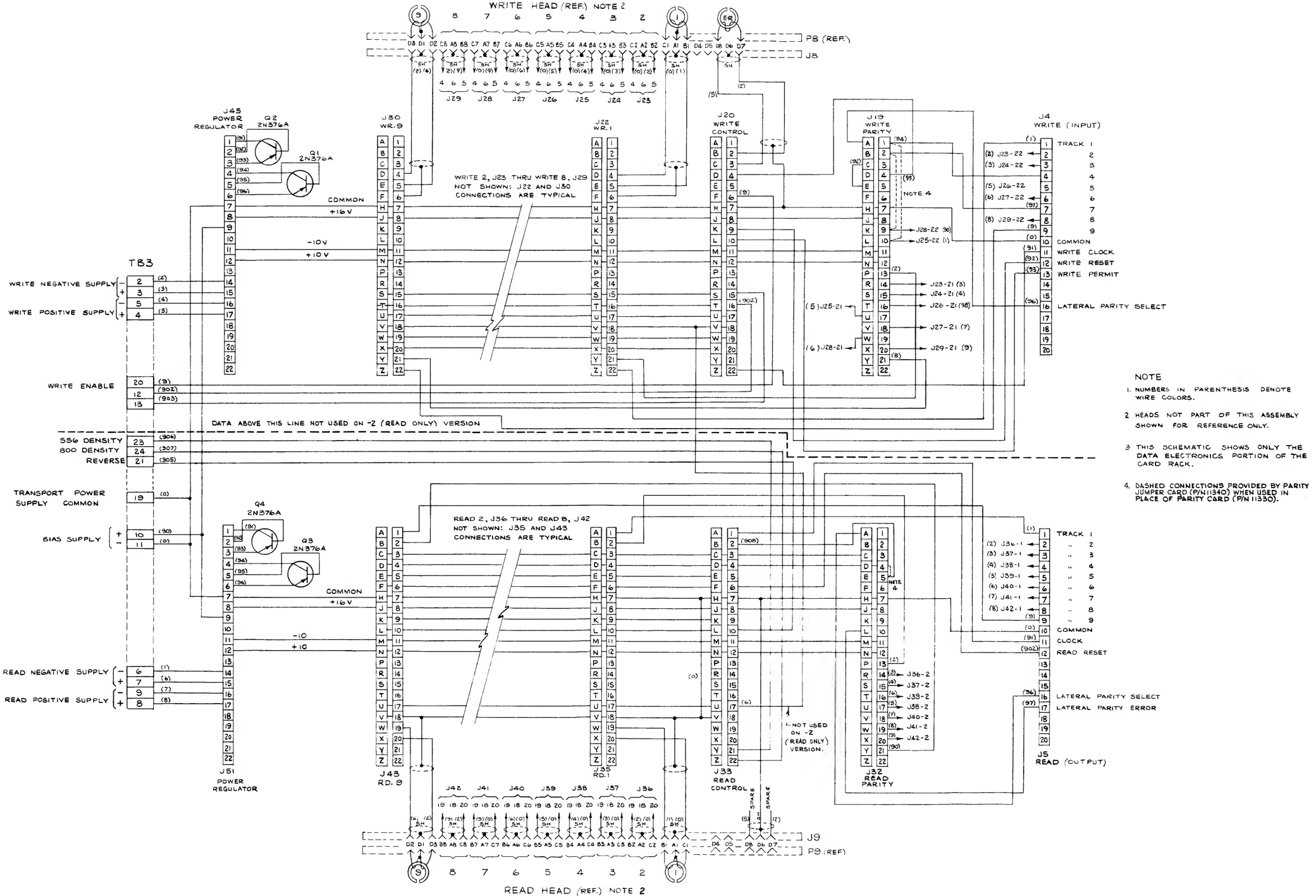
SPEED	C 25	VERSIONS	
		NON-SWITCHER	SWITCHER
25.0 TO 75	.0015	-0	-1
16.7 TO 24.9	.0033	-2	-3
11.1 TO 16.6	.0056	-4	-5
4.95 TO 11.0	.01	-6	-7
3.29 TO 4.94	.015	-8	-9
1.46 TO 3.28	.022	-0	-1
1.00 TO 1.45	.039	-2	-3

11300

11301



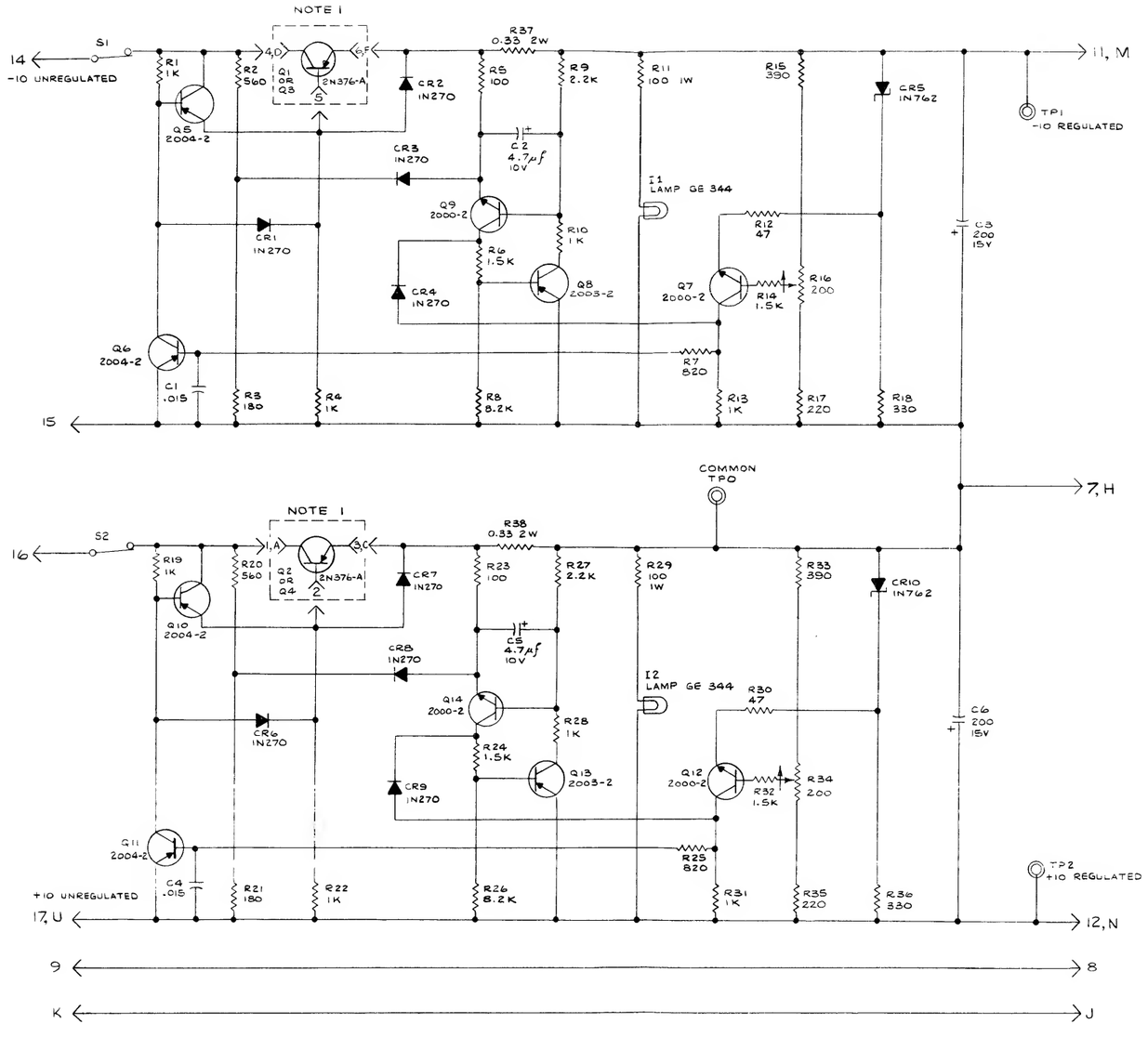
READ CONTROL CARD
(For training purposes only)



NOTE

1. NUMBERS IN PARENTHESIS DENOTE WIRE COLORS.
2. HEADS NOT PART OF THIS ASSEMBLY SHOWN FOR REFERENCE ONLY.
3. THIS SCHEMATIC SHOWS ONLY THE DATA ELECTRONICS PORTION OF THE CARD RACK.
4. DASHED CONNECTIONS PROVIDED BY PARITY JUMPER CARD (P/N 11340) WHEN USED IN PLACE OF PARITY CARD (P/N 11330).

CARD RACK (WRITE/READ)
(For training purposes only)

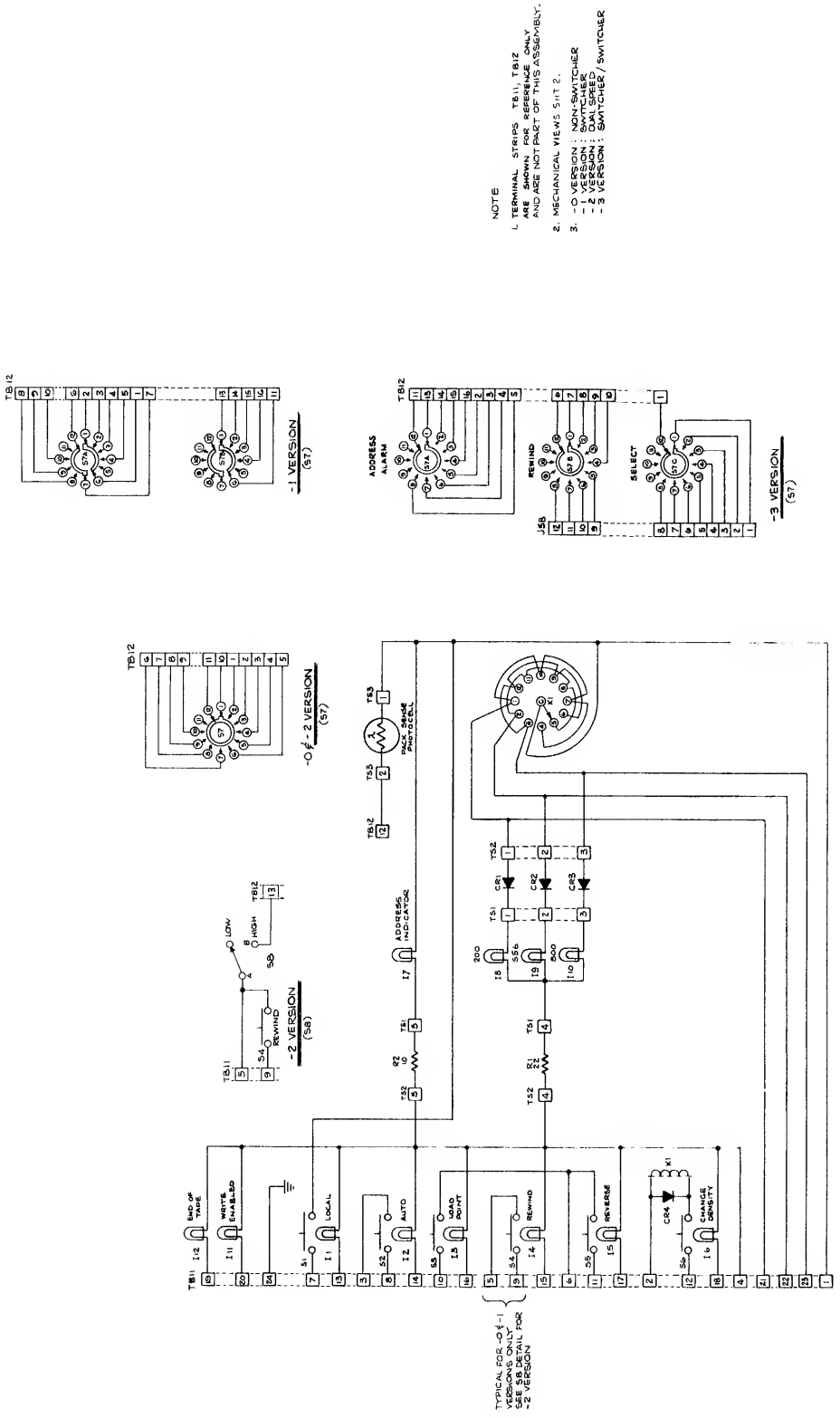


NOTES

1. Q1, 2, 3, 4 NOT PART OF THIS UNIT SHOWN FOR REFERENCE ONLY
2. MARK PART Nº ON 'B' SIDE OF ASSEMBLY
3. UNLESS OTHERWISE NOTED:
   ALL RESISTORS IN OHMS, RATED 1/2 W.
   ALL CAPACITORS IN MICROFARADS

COMPONENT	LAST USED	OMITTED
RESISTOR	R38	
CAPACITOR	C6	
DIODE	CR28	
TRANSISTOR	Q14	Q1,2,3,4

POWER REGULATOR CARD
(For training purposes only)


NOTE
1. TERMINAL STRIPS TB11, TB12 ARE SHOWN FOR REFERENCE ONLY AND ARE NOT PART OF THIS ASSEMBLY.
2. MECHANICAL VIEWS SHT 2.
3. -0 VERSION : NON-SWITCHER
-1 VERSION : SWITCHER
-2 VERSION : DAI SPEED
-3 VERSION : SWITCHER / SWITCHER
-1 VERSION (S7)
-3 VERSION (S7)
-0 & -2 VERSION (S7)
-2 VERSION (S8)
ADDRESS ALARM
REWIND
SELECT
PACK SENSE PROTOCOL
ADDRESS INDICATOR
END OF TAPE
WRITE ENABLED
LOCAL
AUTO
LOAD RQST
REWIND
REVERSE
CHANGE DENSITY
TYPICAL FOR -0 & -1 VERSIONS ONLY SEE S8 DETAIL FOR -2 VERSION

mechanical and electrical adjustment

SECTION V
MECHANICAL AND ELECTRICAL ADJUSTMENT

5-1. VACUUM SYSTEM CHECK AND ADJUSTMENT.

5-2. Equipment required:

a. Vacuum Gauge (0-25 or 0-50 inches of water, full scale).

b. Plastic or rubber tubing (1/4-inch inner diameter).

5-3. Refer to Figure 5-1 for the location of components associated with this adjustment.

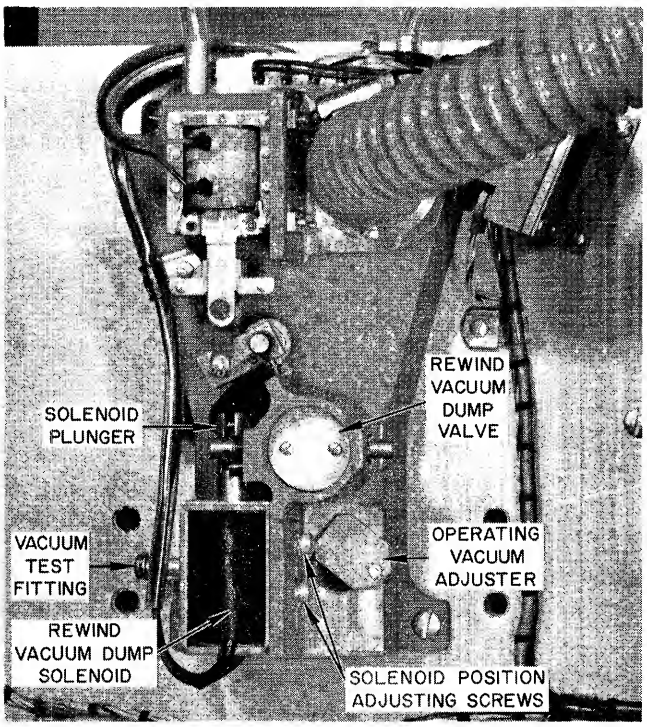


Figure 5-1. Vacuum Valve Adjustment Parts

a. Remove the screw from the vacuum test fitting. Attach the vacuum gauge by means of the 1/4-inch tubing.

b. Thread and load tape onto the unit.

c. Without tape movement the gauge should read 15 inches of water. If this reading is obtained proceed to step "e".

d. Loosen the hex head socket screw securing the vacuum adjuster. Increase or decrease the size of the bleed hole until the proper reading is obtained. Secure the vacuum adjuster by tightening the hex head socket screw.

e. Drive tape Forward until a tape pack of at least 1/2 inch accumulates on the take-up reel.

f. Depress the REWIND button. The gauge should read 10 inches of water. If this reading is not obtained, proceed to step "g". Otherwise, replace the screw in the test fitting.

g. With the vacuum motor running and tape loops in the chambers, press and hold the solenoid plunger all the way into the solenoid. Loosen the solenoid position adjusting screws and move the solenoid vertically until the proper reading is obtained. Secure the solenoid and replace the screw in the test fitting.

5-4. PINCHROLLER ACTUATOR CHECK AND ADJUSTMENT.

5-5. Refer to Figures 5-2 through 5-4 for this adjustment.

5-6. There is an actuator assembly for both Forward and Reverse drive. The following procedure should be performed on both assemblies.

a. Thread and load a scratch tape on the unit. Initiate tape motion and check for a .002-inch clearance between the clapper and the coil housing. If the setting is correct, proceed to step "e".

b. Release the four hold down screws only enough to permit movement of the actuator with some degree of pressure.

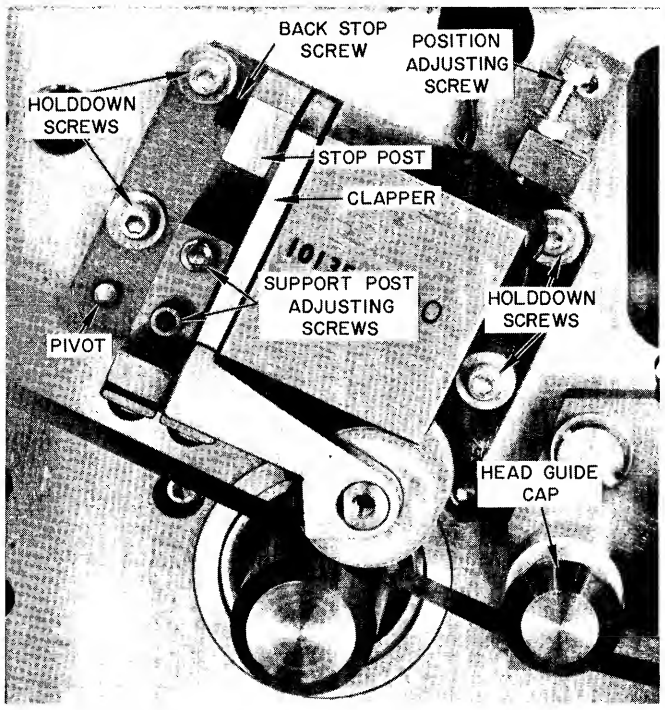


Figure 5-2. Actuator Adjustment Parts

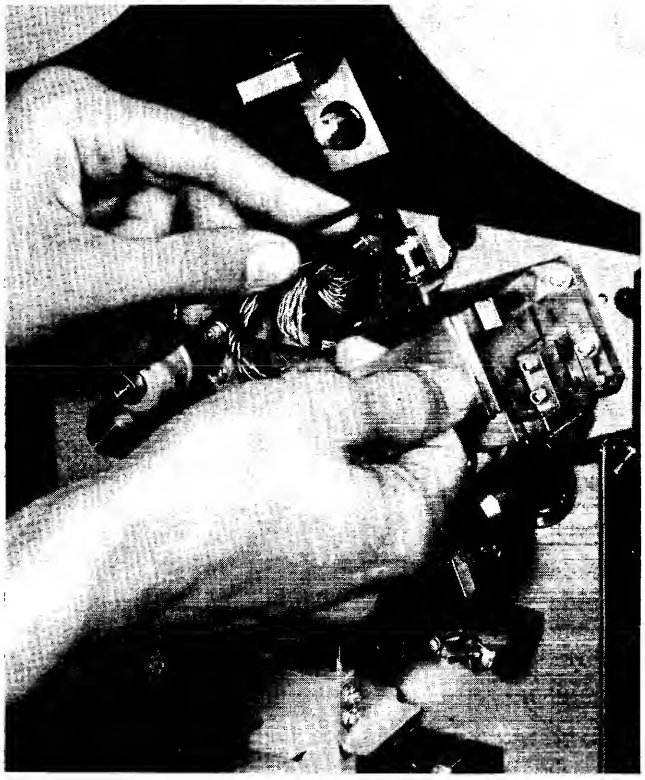


Figure 5-3. Energized Actuator Adjustment

c. Position the actuator while tape is moving, until a .002-inch clearance is obtained. Tighten the hold down screws.

d. Check the gap again and repeat steps "b" and "c" until the proper gap is obtained.

e. Unload the tape from the unit. Establish a gap of .004 inch between the capstan and the pinch roller by adjusting the back stop screw.

5-7. TAPE TRAVEL CHECK AND ADJUSTMENT.

5-8. Refer to Figures 5-2 and 5-5 for this adjustment.

5-9. This procedure must be performed on both the Forward and Reverse assemblies.

a. Remove both head guide caps, taking care not to drop the ceramic guide washers.

a. Thread and load a scratch tape on the unit. Initiate tape motion.

c. Depress the inner spring loaded ceramic washer. If a change in tape travel is noticed, the following steps must be performed. If a change in tape travel is not detected, proceed to step "f".

d. Stop tape motion and loosen the support post adjusting screws. Initiate tape motion. While tape is moving, tighten the adjusting screw nearer the spring until the tape tracks are about 1/16-inch over the edge of the guide.

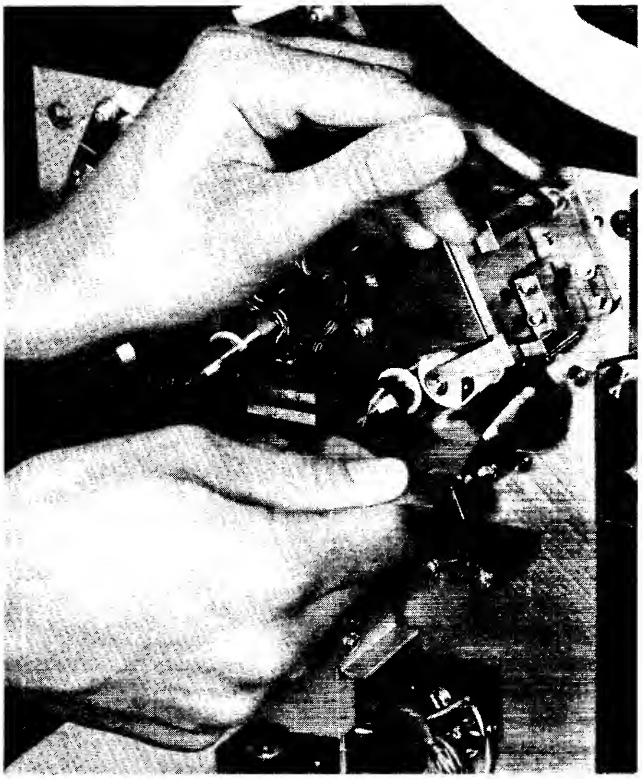


Figure 5-4. De-energized Actuator Adjustment

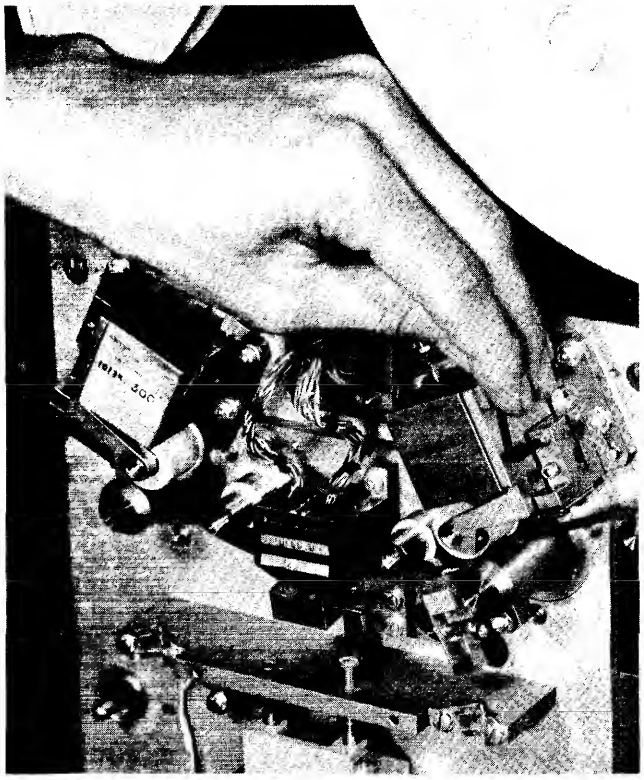


Figure 5-5. Tape Tracking Adjustment

e. Tighten the second adjusting screw until the inner edge of the tape just contacts the inner spring-loaded washer. A few mils of tape should be hanging over the outer edge of the head guide and both screws should be tight and locked against each other.

f. Unload the tape and replace the guide head washers and caps insuring that the smoothest side of the washer is next to the tape edge. If the washers are incorrectly installed, damage to the tape may result.

5-10. HEAD AZIMUTH CHECK AND ADJUSTMENT.

5-11. The azimuth position of the Read/Write head may be checked and adjusted as follows:

a. Thread and load a scratch tape.

b. Without tape motion there should be a visible gap between the capstan and tape and between the tape and pinch roller (both Forward and Reverse assemblies).

c. If necessary, loosen the head assembly screws slightly and rotate the head assembly until the proper clearances are attained.

5-12. REEL BRAKE GAP CHECK AND ADJUSTMENT.

5-13. Before performing this check the unit should be allowed to operate a minimum of 30 minutes.

5-14. There are two immediate indications that brake adjustment is required. They are:

a. During Forward and Reverse tape motion the loops in the vacuum columns edge toward the lower loop alarm sensing holes.

b. During Forward or Reverse tape motion excessive brake "chatter" is heard.

5-15. Another check of the brakes may be made by holding the Transport Switch in the BRAKES position and rotating both reels through a full 360°. If rubbing or binding is detected at any point then the gap must be adjusted.

5-16. Adjust the brakes in the following manner:

a. Unload the tape from the unit. Loosen the set screw holding the brake rotor to the shaft. Tighten the stop nut until a slight amount of drag is detected while the Transport switch is in the BRAKES position.

b. Loosen the stop nut only until brake drag is no longer detected.

c. Tighten the set screw on the brake rotor.

d. Before adjusting the takeup reel brake, remove the two springs from the sides of the drag brake and slide the drag brake plate away from the rotor assembly. Be sure to replace the drag brake assembly after adjusting the reel brake.

5-17. DRAG BRAKE TENSION CHECK AND ADJUSTMENT.

a. Use a spring scale attached to the takeup reel hub with a length of string wrapped around the hub. Pull gently on the scale while holding the Transport switch in the BRAKES position. The reel should barely rotate when the scale indicates 6 ounces.

b. If adjustment of the drag brake is required, alter the tension on the drag brake plate by moving the spring retaining brackets equally on both sides of the brake housing.

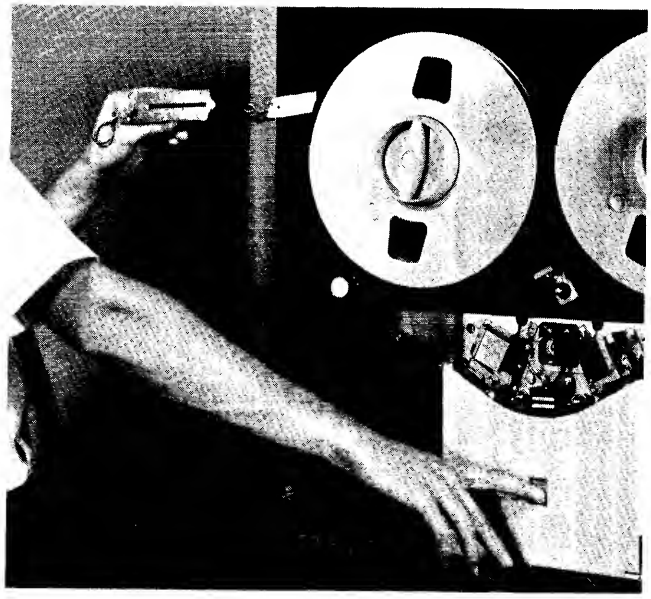


Figure 5-6. Drag Brake Tension Test

5-18. REWIND JOG SETTING CHECK AND ADJUSTMENT.

a. Thread and load tape on the unit. Drive tape Forward until a tape pack of at least 1/2 inch accumulates on the takeup reel.

b. Set oscilloscope time base to 20 milliseconds per centimeter, triggering mode to INT DC and connect the probe on TP1 of the Relay circuit card.

c. Unplug P6 on the vacuum motor exhaust housing located in the rear of the unit.

d. Depress the REWIND pushbutton. The oscilloscope trace should show several square waves. Total cycle time should be 110 msec., 55 msec "on" and 55 msec "off".

e. If necessary, adjust R11 and R15 on the Relay card for the proper time periods.

f. Depress the LOCAL pushbutton and connect P6 on the vacuum exhaust housing.

5-19. PHOTOSENSE CARD ADJUSTMENT.

5-20. Load and thread a tape on the unit. Use a VTVM for the following measurements.

a. Connect meter to chassis ground and TP1 on the Photosense card. Adjust R3 for maximum voltage, but not over +.5 volts DC.

b. Move meter lead to TP2. Adjust R49 for maximum voltage, but not over .5 volts DC.

c. Move meter lead to TP3. Adjust R27 for maximum voltage, but not over .8 volts DC.

d. Position tape at Load Point. TP1 should read +3.0 volts DC minimum.

e. Cover pack Sense lamp. TP3 should read +2.5 volts DC minimum.

f. Position tape at EOT. TP2 should read +3.0 volts DC minimum.

5-21. DATA ELECTRONICS ADJUSTMENTS.

5-22. The 3030 Diagnostic should be used to exercise the tape unit. It may be initialized in the following manner:

a. Load the binary tape using the ABC.

b. Set S.A. = 100B.

c. Set the mag tape data chennal select code in the Switch Register. If a 2115 or 2114 Computer is being used, set switch 15 to a "1". Depress RUN.

d. Set the TTY select code in the Switch Register. If a serial interface is being used, set switch 15 to a "1". Depress RUN.

e. Set the address of the last address (not last available address preceding the loader) in the Switch Register. Depress RUN.

f. The program is now ready for execution.

5-23. READ GAIN ADJUSTMENT.

5-24. There are nine identical Read cards located in the unit. Each card should be adjusted in the same manner.

a. Thread & load a scratch tape (with a Write Register installed) on the unit.

b. Switch the unit to AUTO.

c. Connect the oscilloscope to TP1 on the Read card.

d. Set the computer S.A. = 1000B.

e. Enter 000377B in the Switch Register. RUN.

f. Adjust R12("G") on the Read card for a 6.5V peak-to-peak signal.

g. After all cards have been adjusted set switch 15 to a "1" to halt the program.

h. Switch the unit to LOCAL. Rewind the scratch tape and remove it from the unit.

5-25. FORWARD AND REVERSE READ SKEW ADJUSTMENT.

5-26. Remove the Write Control and Write Power Regulator cards. This will insure that the master alignment tape will not be destroyed. A high speed rewind operation should never be performed while using a master alignment.

a. Thread and load the 800 bpi master alignment tape (without a Write Ring) on the unit. Move tape to load point and switch the unit to AUTO.

b. At the computer, set the S.A. = 1300B. Set switch 3 to a "1". RUN.

c. Connect channel B probe to TP3 of Read card 5. Adjust all Read card FWD potentiometers fully CCW.

d. Adjust the FWD potentiometer on Read card 5 for a 8 μsec negative pulse width.

e. Set the oscilloscope vertical amplifier to the ALT B TRIGGER mode.

f. Connect the channel A probe to TP3 on each of the remaining Read cards in turn. Adjust the FWD potentiometers for a display in phase with that on channel B.

g. On the computer, set switch 3 to a "0" and then switch 5 to a "1".

h. Repeat steps "c" through "f", this time adjusting the REV potentiometers.

i. Halt the program by setting switch 5 to a "0". Remove the master alignment tape and install the Write Control and Write Power Regulator cards.

5-27. At this point, the Read electronics have been aligned to a known standard. It is now necessary to adjust the Write electronics while monitoring the read outputs.

5-28. WRITE SKEW ADJUSTMENT.

a. Adjust R25 on Write card 5 to mid-point (approximately 10 turns from full CCW).

b. Thread and load a scratch tape on the unit. Position the tape at Load Point and switch the unit to AUTO.

c. Set the oscilloscope vertical amplifier to the ALT B TRIGGER mode and connect the channel B probe to TP3 on Read card 5.

d. At the computer, set the S.A. = 1000B and 000377 in the Switch Register. RUN.

e. Connect the channel A probe to TP3 on each of the remaining Read cards in turn. Adjust R25 on each corresponding Write card for a display in phase with that on channel B.

5-29. WRITE BALANCE ADJUSTMENT.

a. Set the oscilloscope for A trace only and INT sync. Connect the channel A probe to TP3 of Read card 1. Adjust the horizontal sweep rate so that 3 character cycles can be observed.

b. If an unbalanced condition exists, the center pulse will have a double image. Adjust R55 on Write card 1 so that the center pulse has a clear and distinct leading and trailing edge.

c. Repeat steps "b" and "c" for each of the remaining tracks.

d. Halt the program by setting switch 15 to a "1".

5-30. CHARACTER GATE ADJUSTMENT.

a. Set the S.A. = 1000B and the Switch Register to 000377.

b. Thread and load a scratch tape. Position the tape at Load Point and switch the unit to AUTO.

c. Depress RUN. When the tape unit goes into Rewind mode halt the computer. Set S.A. = 1300B and switch 3 to a "1".

d. After the tape has been rewound to Load Point, depress PRESET and RUN.

e. Set the oscilloscope mode to A ONLY and connect the channel A probe at TP3 on the Read Control card. Adjust R87 for a 60% positive pulse width.

f. Halt the program by setting switch 3 to an "0" and depressing the HALT button.

5-31. START-STOP TIME CHECK.

5-32. The purpose of the check is to determine if the tape unit is capable of accelerating the tape to full speed within 5 msec of receipt of the drive command and to stop tape movement within 2 msec of removal of the drive command.

a. Set the oscilloscope as follows:

1. Horizontal — 1 msec/cm
2. Sync — EXT Negative
3. Mode — A ONLY

b. Connect the external sync to pin 16 of the Drive card.

c. Connect the channel A probe to TP1 of the Read card for track 5.

d. With the 3030 Diagnostic loaded into the computer, and a scratch tape intalled on the unit, set the S.A. = 1300B and the Switch Register to 000400. RUN.

e. The oscilloscope display should resemble the one in Figure 5-7.

f. Change the oscilloscope to sync EXT Positive.

g. The oscilloscope display should resemble the one in Figure 5-8.

h. Halt the program and remove the tape from the unit.

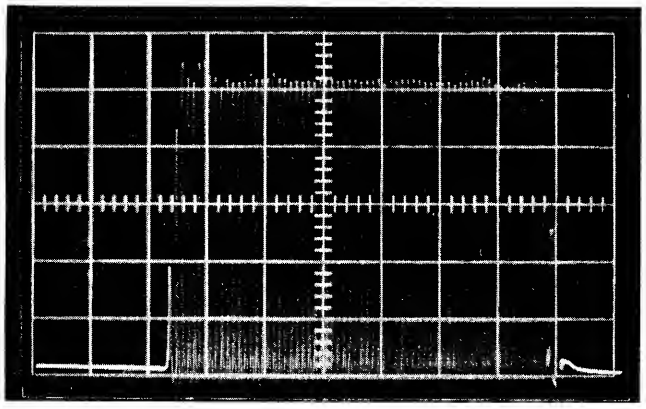


Figure 5-7. Start Characteristics

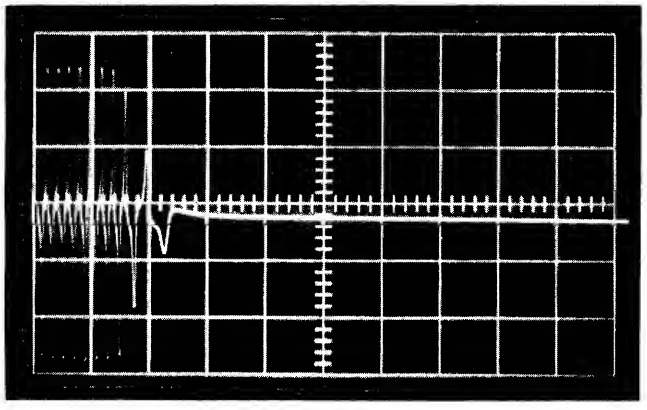


Figure 5-8. Stop Characteristics

HP 12559A interface theory of operation

VI

SECTION VI
HP 12559A INTERFACE THEORY OF OPERATION

6-1. INTRODUCTION.

6-2. The Hewlett-Packard 12559A 9-Track Magnetic Tape Interface Kit provides an interface between an HP 2116, 2115, or 2114 computer and an HP H01-D3030G 9-Track Magnetic Tape Unit. The Interface Kit consists of the following:

a. Mag Tape 1 Interface Card (Part No. 02116-6159).
b. Mag Tape 2 Interface Card (Part No. 02116-6160).
c. Inter-Connecting Cable Assembly (Part No. 02116-6193).
d. SIO Magnetic Tape Unit Driver (Part No. 20331A).
e. BCS Magnetic Tape Unit Driver (Part No. 20022C).
f. HP 3030 Magnetic Tape Test — Binary Tape (Part No. 20433C).

6-3. DESCRIPTION.

6-4. The Mag Tape 1 and 2 cards enable an HP 2116, 2115 or 2114 Computer to record on and read from one-half inch, nine channel, NRZI, IBM compatible magnetic tape with the HP 3030 Magnetic Tape Unit. This unit reads at 200, 556, or 800 bpi and records at 800 bpi density. Tape speed is 75 ips, providing a data transfer rate of 60,000 eight-bit characters per second. The magnetic tape interface cards plug into any two adjacent I/O slots of the computer. Both select codes are encoded with the Mag Tape 1 card assigned the higher priority.

6-5. Data is written in records on the tape with each record having a minimum of 12 characters. An inter-record gap on the tape must be provided to prevent los of information in the event the tape unit is required to stop and/or start between records. The inter-record gap should be a nominal 0.6 inches.

6-6. A character is recorded on channels or tracks across the width of the tape, with each track containing one bit of the character. There are nine tracks, of which eight tracks contain data and one track is used for a parity bit. The parity bit indicates the accuracy of the data and is a logic "0" when the total number of "1" bits in a data character is odd. Conversely, a logic "1" represents an even number of "1" bits in a data character. A parity error occurs only where there is an even number of logical "1's" in the character.

6-7. SPECIFICATIONS.

6-8. Specifications for the 12559A Interface Kit are as follows:

LOGIC LEVELS

	Levels
Write Permit, Write Reset, and Read Reset Control Commands	Negative True, logic "1", -10V logic "0", 0V
Write Clock, Read Clock, and Read Track signals	Positive False, logic "1", 0V logic "0", +10V
Write Track signals	Positive True, logic "1", +10V logic "0", 0V

6-9. Specifications for the Magnetic Tape Unit are as follows:

Number of Tracks	9
Read/Write Speed	75 ips
Density	800 bpi (write)/200, 556 or 800 bpi (read)
Data Transfer Rate	60,000 characters per second max.
Start Time	5 milliseconds bidirectional max.
Stop Time	2 milliseconds bidirectional max.
Reel Capacity (10-1/2-inch diameter reels with IBM compatible hub)	2400 feet of 1/2-inch tape
Rewind Time	< 3 minutes

Magnetic Tape Unit Logic Levels:

Positive True —	logic "1"	+10V
	logic "0"	0V
Positive False —	logic "1"	0V
	logic "0"	+10V
Negative True —	logic "1"	- 10V
	logic "0"	0V
Negative False —	logic "1"	0V
	logic "0"	-10V

Ambient Temperature	32° to 115°F (0° to 46°C)
Relative Humidity	20 to 95%

An auxiliary HP 2160 Power Supply may be necessary for installations which use several I/O devices with high current requirements.

6-10. INSTALLATION.

6-11. Connect the magnetic tape unit to the computer as follows:

a. Turn power off on the computer and the magnetic tape unit.

b. Plug the three cable connectors into the appropriate magnetic tape unit connector.

c. Open the computer for access to the I/O cards.

d. Insert the two interface cards into adjacent I/O slots assigned for the particular computer system. Card No. 02116-6159 must be in the lower numbered select code.

e. Pass the cable connector, which mates with the two interface cards, through the cable slot from the rear of the computer.

f. Slide the connectors onto the cards and close the computer.

6-12. PROGRAMMING.

Note

The two channels used by the magnetic tape unit are labeled DATA and COMMAND for software purposes. The Data channel is the higher priority channel and corresponds to the address slot which the interface card, MAG TAPE 1, is plugged into. The Command channel is the lower priority channel and corresponds to the address slot which the interface card, MAG TAPE 2 is plugged into. Therefore, when referring to software, Command Channel and Data Channel is used in lieu of MAG TAPE 1 and MAG TAPE 2 cards, respectively.

Table 6-1. Interface Cards to Magnetic Tape Unit Connector Pin Assignments

*FROM	TO	SIGNAL	*FROM	TO	SIGNAL
MT1-1	MT2-A	Ground	MT1-M	Spare	
MT1-2	Spare		MT1-N	P1-11	$\overline{\text{End of Tape Status}}$
MT1-3	MT2-3	CCP	MT1-P	Spare	
MT1-4	MT2-4	$\overline{\text{WFM}}$	MT1-R	P1-10	$\overline{\text{Write Enabled Status}}$
MT1-5	MT2-5	WRS	MT1-S	Spare	
MT1-6	MT2-6	$\overline{\text{WRT}}$	MT1-T	P5-12	Read Reset
MT1-7	MT2-7	SRS	MT1-U	Spare	
MT1-8	MT2-8	FWD	MT1-V	P4-13	Write Enable
MT1-9	MT2-9	REV	MT1-W	Spare	
MT1-10	MT2-10	EOR	MT1-X	P1-3	Reverse Drive
MT1-11	Spare		MT1-Y	Spare	
MT1-12	Spare		MT1-Z	P1-5	Unload
MT1-13	P1-8	$\overline{\text{Auto Status}}$	MT1-AA	Spare	
MT1-14	Spare		MT1-BB	MT1-24	Ground
MT1-15	P1-15	Rewind Status			
MT1-16	Spare		MT2-1	Spare	
MT1-17	P1-9	$\overline{\text{Load Point Status}}$	MT2-2	Spare	
MT1-18	Spare		MT2-3	MT1-3	CCP
MT1-19	P4-12	Write Reset	MT2-4	MT1-4	$\overline{\text{WFM}}$
MT1-20	Spare		MT2-5	MT1-5	WRS
MT1-21	P1-2	Forward Drive	MT2-6	MT1-6	$\overline{\text{WRT}}$
MT1-22	Spare		MT2-7	MT1-7	SRS
MT1-23	P1-4	Rewind Drive	MT2-8	MT1-8	FWD
MT1-24	P1-36	Ground	MT2-9	MT1-9	REV
	MT2-BB	Ground	MT2-10	MT1-10	EOR
	MT1-BB		MT2-11	Spare	
MT1-A	Spare		MT2-12	Spare	
MT1-B	Spare		MT2-13	P5-2	Read Track 2
MT1-C	MT2-C	A2	MT2-14	P5-8	Read Track 8
MT1-D	MT2-D	$\overline{\text{SPC}}$	MT2-15	P5-1	Read Track 1
MT1-E	MT2-E	ADSD	MT2-16	P5-9	Read Track 9
MT1-F	MT2-F	ACI	MT2-17	P5-3	Read Track 3
MT1-H	MT2-H	$\overline{\text{DTF}}$	MT2-18	P5-5	Read Track 5
MT1-J	MT2-J	SFB	MT2-19	P5-6	Read Track 6
MT1-K	MT2-K	$\overline{\text{CLR}}$	MT2-20	P5-7	Read Track 7
MT1-L	MT2-L	WTC	MT2-21	P5-4	Read Track 4

Note: MT1 and MT2 refer to Magnetic Tape 1 and Magnetic Tape 2 Interface cards, respectively.

Table 6-1. Interface Cards to Magnetic Tape Unit Connector Pin Assignments (Continued)

*FROM	TO	SIGNAL
MT2-22	P5-11	Read Clock
MT2-23	Spare	
MT2-24	MT2-1	Bus Wire
MT2-24	MT2-A	Ground
MT2-24	P5-10	Ground
MT2-24	MT2-BB	Ground
MT2-A	MT1-1	Ground
MT2-B	Spare	Ground
MT2-C	MT1-C	A2
MT2-D	MT1-D	$\overline{SPC}$
MT2-E	MT1-E	ADSD
MT2-F	MT1-F	ACI
MT2-H	MT1-H	$\overline{DTF}$
MT2-J	MT1-J	SFB
MT2-K	MT1-K	$\overline{CLR}$
MT2-L	MT1-L	WTC
MT2-M	Spare	
MT2-N	Spare	
MT2-P	P4-2	Write Track 2
MT2-R	P4-8	Write Track 8
MT2-S	P4-1	Write Track 1
MT2-T	P4-9	Write Track 9
MT2-U	P4-3	Write Track 3
MT2-V	P4-5	Write Track 5
MT2-W	P4-6	Write Track 6
MT2-X	P4-7	Write Track 7
MT2-Y	P4-4	Write Track 4
MT2-Z	P4-11	Write Clock
MT2-AA	Spare	
MT2-BB	P4-10	Ground
MT2-BB	MT2-24	Ground
P1-1	P1-36	Ground
P1-2	MT1-21	Forward Drive
P1-3	MT1-X	Reverse Drive
P1-4	MT1-23	Rewind Drive
P1-5	MT1-Z	Unload Drive
P1-6	Spare	
P1-7	Spare	
P1-8	MT1-13	$\overline{\text{Auto Status}}$
P1-9	MT1-17	$\overline{\text{Load Point Status}}$
P1-10	MT1-R	$\overline{\text{Write Enabled Status}}$
P1-11	MT1-N	$\overline{\text{End of Tape Status}}$
P1-12	Spare	
P1-13	Spare	
P1-14	Spare	
P1-15	MT1-15	$\overline{\text{Rewind Status}}$
P1-16	Spare	
P1-17	Spare	
P1-18	Spare	
P1-19	Spare	
P -20	Spare	
P1-21	Spare	
P1-22	Spare	
P1-23	Spare	

*FROM	TO	SIGNAL
P1-24	Spare	
P1-25	Spare	
P1-26	Spare	
P1-27	Spare	
P1-28	Spare	
P1-29	Spare	
P1-30	Spare	
P1-31	Spare	
P1-32	Spare	
P1-33	Spare	
P1-34	Spare	
P1-35	Spare	
P1-36	P1-1,	
P1-5	MT1-24	Ground
P4-1	MT2-S	Write Track 1
P4-2	MT2-P	Write Track 2
P4-3	MT2-U	Write Track 3
P4-4	MT2-Y	Write Track 4
P4-5	MT2-V	Write Track 5
P4-6	MT2-W	Write Track 6
P4-7	MT2-X	Write Track 7
P4-8	MT2-R	Write Track 8
P4-9	MT2-T	Write Track 9
P4-10	MT2-BB	Ground
P4-11	MT2-Z	Write Clock
P4-12	MT1-19	Write Reset
P4-13	MT1-V	Write Permit
P4-14	Spare	
P4-15	Spare	
P4-16	Spare	
P4-17	Spare	
P4-18	Spare	
P4-19	Spare	
P4-20	Spare	
P5-1	MT2-15	Read Track 1
P5-2	MT2-13	Read Track 2
P5-3	MT2-17	Read Track 3
P5-4	MT2-21	Read Track 4
P5-5	MT2-18	Read Track 5
P5-6	MT2-19	Read Track 6
P5-7	MT2-20	Read Track 7
P5-8	MT2-14	Read Track 8
P5-9	MT2-16	Read Track 9
P5-10	MT2-24	Ground
P5-11	MT2-22	Read Clock
P5-12	MT1-T	Read Reset
P5-13	Spare	
P5-14	Spare	
P5-15	Spare	
P5-16	Spare	
P5-17	Spare	
P5-18	Spare	
P5-19	Spare	
P5-20	Spare	

6-13. All instructions require tape motion except for the CLEAR (CLR) command. This command does not require any participation on the part of the tape unit. Commands and status information are transferred through the A- or B-Register to the Command Channel with standard I/O instructions. Data is transferred through the Data Channel to or from the A- or B-Register. The Command Flag and Interrupt signals indicate the completion of operations requiring tape motion. If the Control FF in the Command Channel is not set by an STC (Set Control) instruction, interrupt requests from the magnetic tape unit will be inhibited.

6-14. PROGRAM COMMANDS.

6-15. Figure 6-1 identifies the functions to be performed by the magnetic tape unit when the respective bit of the 8-bit command word is a logic "1". The WRITE command bit (b_3) and the MOTION bit (b_0) result in forward motion of the tape during a write operation so that the FORWARD bit (b_1) need not be programmed. Table 6-2 lists the command bit combinations required for the listed magnetic tape unit operations.

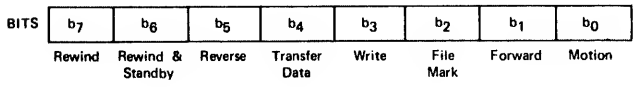


Figure 6-1. Eight-Bit Command Word

Table 6-2. Encoded Magnetic Tape Unit Commands

BIT COMBINATIONS	OCTAL	MNEMONIC	COMMAND
$b_0b_3b_4$	31	WCC	Write Characters
$b_0\ b_1\ b_4$	23	RCC	Read Characters
$b_0\ b_3$	11	GAP	Write 3" Blank Tape
$b_0\ b_1$	3	FSR	Forward Space Record
$b_0\ b_5$	41	BSR	Back-Space Record
$b_0\ b_7$	201	REW	Rewind
$b_0\ b_6$	101	RWS	Rewind and Standby
$b_7\ b_6$	300	CLR	Clear
$b_0\ b_2\ b_3\ b_4$	35	WFM	Write File Mark

6-16. WRITE CHARACTERS (WCC). The Write Character operation (WCC) initiates forward motion and sets up the necessary conditions for writing. This command prepares the Data Channel for each character to be written on tape. Only bits Ø through 7 of the word loaded into the Data Channel are written on tape. Computer words written on tape have the following bit and track assignments (P denotes Parity bit):

BIT	0	1	2	3	4	5	6	7	P
TRACK	2	8	1	9	3	5	6	7	4

6-17. A Clear Control (CLC) instruction immediately after the last character of a record is written, performs the following:

a. Initiates an end-of-record sequence by writing Cyclic Redundancy Check and Logitudinal Redundancy Check Characters.

b. Provides an inter-record gap.

c. Stops tape motion.

A typical programming sequence is as follows:

```
START  CLC  ØC        DISABLE ALL I/O & TURN OFF INTER.
       LDA  COUNT
       STA  TEMP      INITIALIZE COUNTER FOR 12 CHAR.
       LIB  1         INPUT DATA TO BE WRITTEN BITS Ø-7
       LDA  CMND
       OTA  COMCH     OUTPUT WRITE COMMAND TO CMND. CH.
01A    SFS  DATCH
       JMP  *-1       TEST FOR DATA CH. FLAG
       OTB  DATCH     OUTPUT DATA TO DATA CHANNEL
       ISZ  TEMP      INCREMENT CHARACTER COUNTER
       JMP  01A
       CLC  DATCH,C   CLEAR DATA TRANSFER FF
       LIA  1         INPUT SWITCH REGISTER
       SSA            SKIP IF BIT 15 = Ø CONTINUE OPER.
       HLT  77B       NORMAL HALT
       SFS  COMCH     CHECK COMMAND CHANNEL FLAG FOR
       JMP  *-1       END OF OPERATION
       LIA  COMCH     INPUT STATUS
       AND  MASK      EXTRACT EOT STATUS BIT
       SZA, RSS       SKIP IF EOT DETECTED
       JMP  START     REPEAT
       LDA  REW
       OTA  COMCH,C   OUTPUT REWIND COMMAND
       SFS  COMCH     CHECK COMMAND CHANNEL FLAG
       JMP  *-1       FOR END OF OPERATION
       JMP  START
COUNT  OCT  177764    NEGATIVE 12 DECIMAL
CMND   OCT  31        WRITE COMMAND
REW    OCT  2Ø1       REWIND COMMAND
MASK   OCT  ØØØØ4Ø
TEMP   OCT  Ø
```

NOTE: DATCH = LOWER SELECT CODE
COMCH = HIGHER SELECT CODE

6-18. The read after write parity checks continue after writing has been completed. Both the vertical and longitudinal parity are checked. When tape motion stops the Command Flag FF is set and the Command Channel is ready for the next operation.

6-19. READ CHARACTERS COMMAND (RCC). The Read Character operation initiates forward motion and sets up the necessary conditions for reading. A Read Clock Signal sets the Data Flag FF each time a character is read from the tape. Data may be loaded into bits Ø through 7 of the A- or B-Register with a Load or Merge instruction. Forward motion continues until an inter-record gap is detected. After forward motion ceases, the Command Flag FF sets and the Command Channel is ready for the next command. Records of less than 12 characters long are illegal.

6-20. GAP Command (GAP). The Gap operation erases 3 inches of tape. This is used for spacing over damaged sections of tape or for file gap generation. The Command Flag FF sets when the forward motion ceases and frees the Command Channel for the next command.

6-21. FORWARD SPACE RECORD (FSR) and BACK SPACE RECORD (BSR) Command. The FSR operation spaces the tape forward until an inter-record gap is detected. The BSR operation moves the tape backward until an inter-record gap or Load Point is detected. The Command Flag FF is set after tape motion has ceased and the Command Channel is ready for the next command.

6-22. REWIND COMMAND (REW). The Rewind operation rewinds the tape and positions it at the Load Point. The Command Flag FF is set when the operation is completed and the Command Channel is ready for the next command.

6-23. REWIND AND STAND-BY COMMAND (RWS). The Rewind and Stand-by operation positions the tape at Load Point and switches the tape unit to LOCAL mode.

6-24. CLEAR COMMAND (CLR). The Clear operation resets the Command Channel and Data Channel to the preset state. If the magnetic tape unit is rewinding, the operation is completed. This command is also executed by pressing the computer PRESET switch. When all motion has ceased and the magnetic tape unit is not in the LOCAL mode, the Command and Data Channels are made ready to accept Data and the Command Flag FF is set. In all cases the system will not be ready for additional commands until at least 5 milliseconds after a Clear Command is issued.

6-25. WRITE FILE MARK COMMAND (WFM). The Write File Mark operation writes the File Mark Character (a logic "1" bit in tracks 2, 3 and 8) and writes the accompanying longitudinal redundancy check character. When the operation is completed, forward motion ceases, the Command Flag FF is set, and the Command Channel is made ready for the next operation. A Cyclic Redundancy Check Character is not written in a File Mark record.

6-26. NINE BIT STATUS WORD.

6-27. The magnetic tape unit provides nine bits of status information to the computer. Status information corresponding to the individual bits of the status word is shown in Figure 6-3. All bits of the status word except BUSY (Bit 0), EOT (Bit 5), BOT (Bit 6) and $\overline{\text{WRITE ENABLED}}$ (Bit 2) are reset to a logic "0" when a clear command is given, or a command resulting in tape motion is accepted by the tape unit. The EOT, BOT and $\overline{\text{WRITE ENABLED}}$ bits are reset to a logic "0" when the conditions they represent are no longer true. The BUSY bit is reset upon completion of any operation. The nine bit status word may be examined at any time with a LIA or LIB instruction with the Command Channel Select Code.

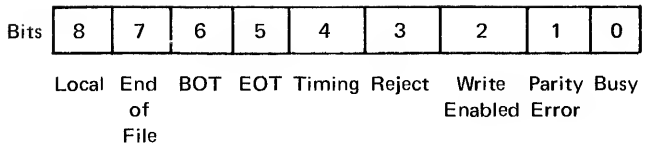


Figure 6-2. Status Word Format

6-28. BUSY (Bit 0). This bit is a logic "1" when the tape is in motion or the magnetic tape unit is in the LOCAL mode. If bit 0 is a logic "0", the Command and Data Channels are ready to accept a command.

6-29. PARITY ERROR (Bit 1). This bit is set to the "1" state if a vertical or longitudinal Parity Error occurs during a Read or Write operation. Parity is not checked on Forward Space Record and Back Space Record operations. The longitudinal parity of the entire record is checked on all Read operations. Vertical parity is checked only during the data transfer portion of a record.

6-30. WRITE ENABLED (Bit 2). This bit is a logic "1" if the Write Ring is not installed in the tape reel. The Write Ring must be inserted in the tape reel before a Write operation can be performed.

6-31. REJECT (bit 3). A command will be rejected and bit 3 set to a logic "1" if tape motion is requested and the I/O interface cards are busy, backward tape motion is requested and the tape is at Load Point, or a Write command is given and the tape reel does not have a Write Ring.

6-32. TIMING (bit 4). This bit is set if the Data Channel Flag FF has not been reset before the next character is transferred by the Data Channel.

6-33. END-OF-TAPE (bit 5). This bit is set when the End-of-Tape reflective marker is sensed while the tape is moving forward. Bit 5 remains set until a REWIND command is given.

6-34. BEGINNING-OF-TAPE (bit 6). This bit is a logic "1" while the Beginning-of-Tape reflective marker is under the photo sense head.

6-35. END-OF-FILE (bit 7). This bit is a logic "1" when a one character File Mark (23 octal) record is detected while reading, forward spacing or backward spacing. It is also set when a File Mark record is written.

6-36. LOCAL (bit 8). This bit is a logic "1" when the magnetic tape unit is in the LOCAL mode.

6-37. NRZI RECORDING.

6-38. The Non Return to Zero Invert (NRZI) technique records a "1" bit with a flux reversal. This means that the tape is magnetized in one direction in all tracks during a gap. Everytime a "1" is to be recorded in a particular track, the magnetic tape head current is

reversed and the tape track is magnetized in the opposite direction. Since the nine track tape uses odd vertical parity there is always at least one flex reversal per character across the tape. Clock tracks are not necessary.

6-39. TRACK SPACINGS AND BIT LOCATIONS.

6-40. The nominal spacing from the center of one track to the center of the next track is 0.055 inch. The nominal bit width is 0.048 inch, with the bits on the outer edge coming within 0.029 inch of the edge. Since the bits on the outer edge of the tape are less reliable, the least used bits were placed on the outer edges. Figure 6-3 illustrates the spacing, track location and corresponding HP computer and IBM computer bit numbers.

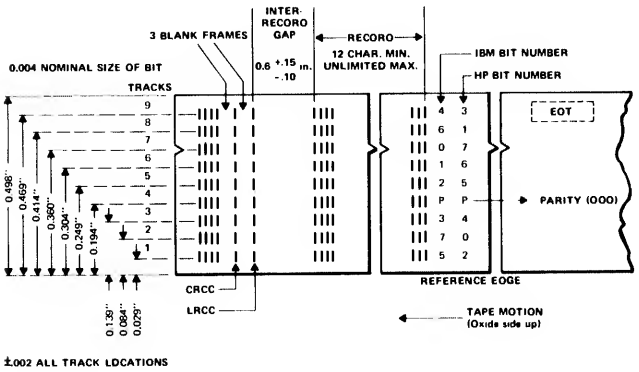


Figure 6-3. Tape Format

6-41. RECORD AND GAP LENGTHS.

6-42. A record must contain at least 12 data characters. Each record contains a data block, Cyclic Redundancy Check Character (CRCC), and a Longitudinal Redundancy Check Character (LRCC). The Cyclic Redundancy Check Character is spaced four characters from the end of the data block. The Longitudinal Redundancy Check Character is spaced four characters past the Cyclic Redundancy Check Character. Between each record is a 0.6 inch nominal record gap.

6-43. VERTICAL PARITY.

6-44. Each nine bits recorded across the width of the tape include eight data bits and a parity bit. Since the number of logic "1's" in the nine bits are always odd, the parity is odd.

6-45. CYCLIC REDUNDANCY CHECK CHARACTER.

6-46. Each IBM compatible record has a Cyclic Redundancy Check Character (CRCC) which is generated during data transfer. The Cyclic Redundancy Check Character, when used in conjunction with software, provides an effective means of detecting the loss of data within a record. It is possible to not only detect the loss, but to restore the data to its original configuration. The CRCC is generated in compliance with the following rules: If the CRC bit ∅ is equal to a logic "0", then a half add of all data bits and CRC bits is performed; after the half add is complete, the CRC character is then rotated right one position; if the CRCC bit ∅ is equal to a logic "1" then an addition with a carry into CRCC bits 3, 4, 5, and 6 is accomplished. CRCC bits 0, 1, 2, 7, and 8 are only half added. At the completion of the add precess the CRC character is rotated right one position. Figure 6-4 shows the relationship between the CRCC bits and the data bits during the addition phase of the CRCC generation. When the CRCC is to be written on tape, all bits except 3 and 5 are inverted and gated to the data lines. A vertical parity bit is not generated for the CRC character. If an even number of characters have been written in the record then the CRC character will have an odd vertical parity. If an odd number of characters have been written, then the vertical parity of the CRC character is even.

DATA	7	6	5	4	3	2	1	0	P
CRCC	8	7	6	5	4	3	2	1	0

6-4. Data-CRCC Bit Relationship

6-47. LONGITUDINAL REDUNDANCY CHECK CHARACTER.

6-48. The last character in a record is the Longitudinal Redundancy Check Character and is nine bits wide. The Longitudinal Redundancy Check Character (LRCC) ensures that the number of logic "1's" in each track is even. A vertical parity bit is not generated for the LRCC, since this would defeat the purpose of the LRCC. The LRCC is sometimes referred to as the Longitudinal Parity Character.

6-49. SIGNALS REQUIRED BY THE TAPE UNIT (Refer to Figure 6-5).

6-50. FORWARD. When this negative true signal is true, the forward actuator of the tape unit is pressed against the capstan which moves the tape from the supply reel, past the Read/Write head, toward the take-up reel at a speed of 75 inches per second.

6-51. REVERSE. When this negative true signal is true, the reverse actuator of the tape unit is pressed against the capstan which moves the tape from the take-up reel, past the Read/Write head, toward the supply reeel at a speed of 75 inches per second.

6-52. REWIND. When this negative true signal is true, the tape is wound on to the supply reel until a Load Point marker is detected. Depending upon the amount of tape on the take-up reel, the tape is moved to the Load Point at 75 inches per second, or removed from the vacuum chambers and rewound at high speed. The Rewind operation is controlled by the magnetic tape unit. The Command Channel Flag FF is set upon completion of the operation.

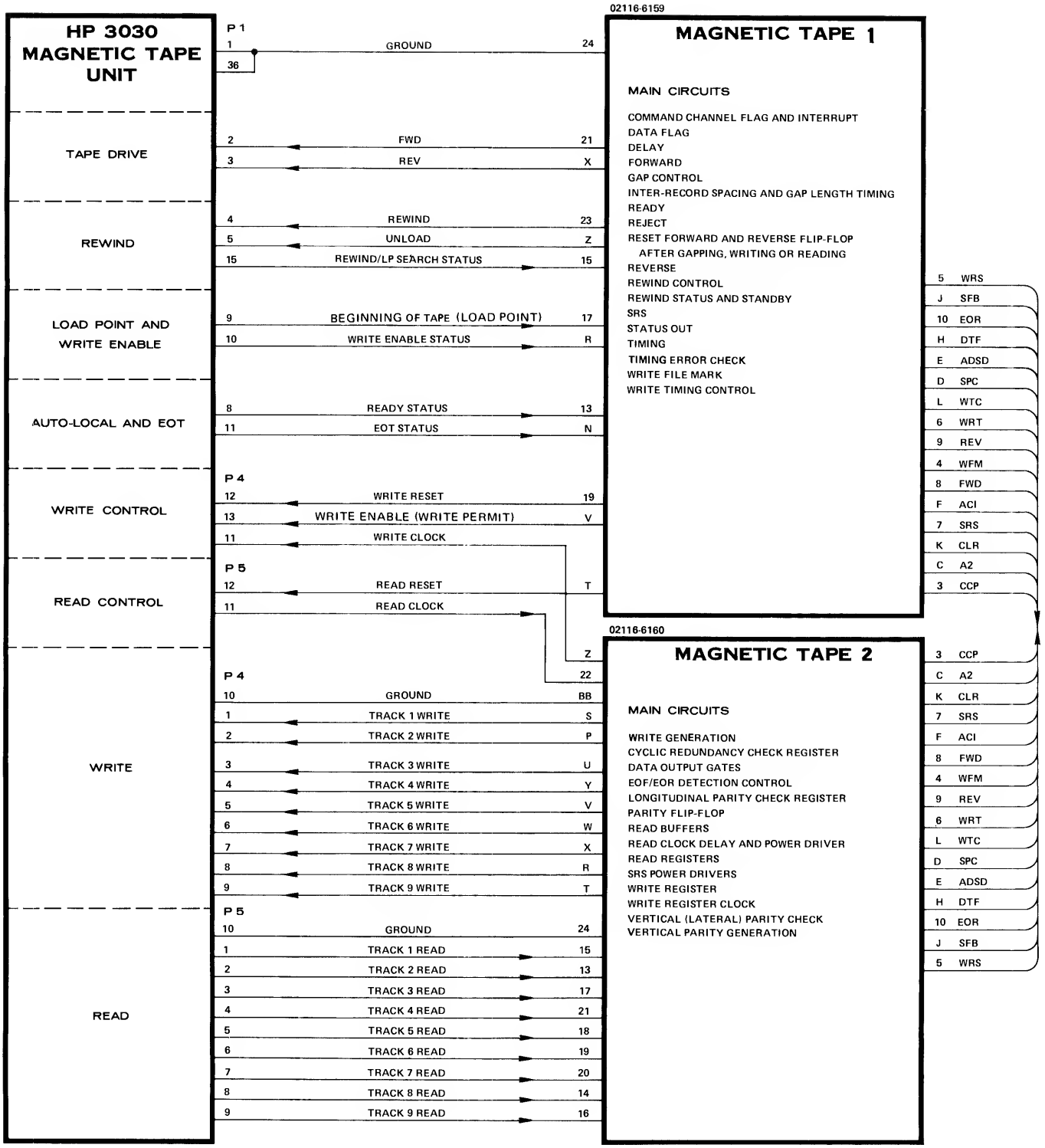


Figure 6-5. HP Computer Interface to H01-D3030G Magnetic Tape Unit

6-53. UNLOAD. When this negative true signal is true, the magnetic tape unit switches to the LOCAL mode and rewinds the tape to the Beginning-of-Tape marker.

6-54. WRITE TRACKS. Each write track driver controls the bit written in that track on the tape during a Write operation. The write track singals are positive true.

6-55. WRITE CLOCK. The positive false Write Clock signal provides the magnetic tape unit with the appropriate data rate. An internal tape unit strobe is triggered on the trailing edge of the Write Clock.

6-56. WRITE RESET. When this negative true signal is true, the write cards in the magnetic tape unit are held in the "0" state. When this signal is false, the write cards in the magnetic tape unit are enabled for switching.

6-57. WRITE PERMIT (WRITE ENABLE). When this negative true signal is true, current flows in the write head so the magnetic tape can be magnetized.

6-58. READ RESET. When this negative true signal is true, the magnetic tape unit read cards are held in the reset state in order to space over gaps.

6-59. SINGALS SUPPLIED BY THE TAPE UNIT.

6-60. READY. This positive false signal is true when the magnetic tape unit is in the AUTO mode and false when the magnetic tape unit is in the LOCAL mode. When the tape unit is in the AUTO mode, the computer can write or read from the unit. When the unit is in the LOCAL mode, the magnetic tape will not move and the writing or reading of data is inhibited.

6-61. LOAD POINT STATUS. When this positive false signal is true, the tape is positioned so that the reflective Beginning-of-Tape marker is under the photo cell.

6-62. WRITE ENABLED STATUS. This positive false signal is true when there is a Write Ring in the tape supply reel.

6-63. END-OF-TAPE STATUS. This positive false signal is true from the time the photocell detects a reflective End-of-Tape marker until the tape unit receives a Rewind command.

6-64. REWIND STATUS. This positive false signal is true during a Rewind operation.

6-65. READ CLOCK. The positive false Read Clock is a data rate pulse generated from an "OR" function of all read cards in the tape unit. A read Clock occurs each time a single data bit is detected by the tape unit.

6-66. READ TRACKS. The positive false Read Data is applied to the Mag Tape 2 Interface Card.

6-67. THEORY OF OPERATION.

6-68. The 3030 interface consists of two physical cards, MAG TAPE 1 (02116-6159) and MAG TAPE 2 (02116-6160). The major function of the MAG TAPE 1 card is to provide timing and control signals to the tape unit and to the MAG TAPE 2 card. It accepts the command words from the computer, status signals from the unit, provides status bits to the computer and controls End-of-Operation interrupts.

6-69. The MAG TAPE 2 card performs data handling functions. It buffers the Write Data characters, generates the proper parity, generates the Cyclic Redundancy Check Character and provides write timing signals to the tape unit. During a Read operation, the data is buffered, the parity is checked and End-of-Record (EOR) and End-of-File (EOF) detection is performed.

6-70. Manu signals are transmitted between the two cards. This is accomplished through the 48 Pin Connectors (refer to Table 6-1).

6-71. WRITE OPERATION. Under program control a Write command (31 octal) is issued to the Command channel. In the command word bit 0 is a logic "1" indicating motion, bit 3 is a logic "1" indicating a Write operation, and bit 4 is a logic "1" indicating there will be a transfer of data. The motion bit is applied to the MAG TAPE 1 card at Pin 35. It is buffered through MC55C & D and applied to NAND gate MC56B. Here a check is made to determine if the tape unit is in LOCAL mode and if the interface is ready to accept the new command. If the unit is in LOCAL mode or the interface is not ready to accept the command, then the Reject FF (MC66B) will be set providing a Reject status to the computer. If the unit is in AUTO mode and the interface is ready, then a motion level (MOT) is generated at MC54D. The motion level is applied to NAND gate MC62B. If the Write bit in the command word is a "1" and a Write Ring is installed on the supply reel mounted on the tape unit, then the NAND gate MC62B outputs a logic "0" which is applied to the Write FF causing it to become set. The MOT level is also applied to MC53D where it is ANDed together with the set output of the Write FF. MC53F inverts the level and applies it to MC75 and to the direct set input to the Forward FF MC115A. The Forward FF now being set provides a Forward Drive signal through Q5 to the tape unit. The signal applied to Pin 6 of MC75 causes the generation of the signal Start Reset (SRS). This signal accomplishes many different things simultaneously and serves the function of setting the control circuitry to the initial state. The SRS Signal accomplishes the following:

a. Resets the divide-by-two counter MC102A.

b. Resets the divide-by-five counter MC102B, C & D.

c. Clocks the Ready FF MC22A to the reset state.

d. Sets the 3" Gap Control FF (MC116A) if the tape is positioned at Load Point. If MC116A becomes set, Write Timing Control is disabled at MC86D and the clearing of the Read Reset FF (MC115B) is disabled at gate MC117C. This will allow 3.5 inches of tape to be moved prior to attempting to write data.

e. Resets the Timing FF (MC43) through gates MC42B and MC42C.

f. ANDed with the Data Transfer bit (Bit 4 of the command word) at MC32D. The output of which directly sets the Data Transfer FF MC22B and generates the signal $\overline{SPC}$.

g. The $\overline{SPC}$ signal from pin D of the MAG TAPE 1 card is applied to pin D of the MAG TAPE 2 card, where it will set the Parity Control FF (MC92C).

h. Resets the Data Flag Buffer FF (MC24B) through gates MC34B, MC34C, MC23D and MC23C.

i. Resets the Data Flag FF (MC35A) through MC34B and MC34C.

j. Resets Command Flag Buffer FF (MC24A) through MC36D, MC36F, MC44A and MC44B.

k. Resets the Command Flag FF (MC45D) through gates MC36D and MC36F.

l. The SRS signal is transmitted to the MAG TAPE 2 card through pin 7, where it is applied to NAND gates MC47A and MC47B, and resets the divide-by-16 counter (MC63).

m. Resets the Cyclic Redundancy Check Character Register which is made up ot MC25A and B, MC35A and B, MC45A and B, MC55A and B, and MC65A.

n. Resets the Cyclic Redundancy Character FF (MC52A).

o. Resets the Write Clock Control FF (MC32).

p. Sets the Write Reset FF (MC33)

q. Resets the Parity FF (MC82).

r. Resets the Longitudinal Redundancy Check Character Register which consists of MC75A and B, MC76A and B, MC85A and B, MC95A and B, and MC102B.

s. Resets the Read Record FF (MC102A).

t. Resets the End-of-Record Control FF (MC52B).

u. Resets the End-of-File FF (MC62A).

v. Resets the End-of-Record FF (MC65B).

6-72. On the MAG TAPE 1 card the Write Reset level and the Write level are ANDed together at MC94D, inverted by MC94F and MC104, then ANDed with the Forward signal from the Forward FF at MC94B. The output of MC94B is inverted by MC94C. The output of MC94C removes the reset level from the spacing counters consisting of MC93, MC103, and MC113A, C and D. If the 3" Gap Control FF (MC116A) was set due to the fact that the tape was positioned at Load Point it will be cleared by the output of a gate MC117B and Clock Control Pulse after 3-1/2 inches of tape have been moved. It should be noted at this point that the Clock Control Pulse is a 60 kilohertz signal and determines the data transfer rate. Once the 3" Gap Control FF has become reset, Writing Timing Control is again enabled at MC86D and resetting of the Read Reset FF will again be enabled at MC117C. The Read Reset FF (MC115B) will be cleared on receipt of the next A2 timing pulse. This will remove the Read Reset signal to the tape unit allowing the read circuitry to detect the presence of data on the tape. Even though a Write operation is being executed, the unit is capable of reading data immediately after it has been written. When the next 200 microsecond Spacing Clock Pulse (SCP) is generated, Write Timing Control (WTC) is enabled through pin L of the MAG TAPE 1 card to pin L of the MAG TAPE 2 card. When the Clock Control Pulse is generated, the Write Clock Control FF (MC32) becomes set enabling write character timing through gates MC23C, MC23D and transistor Q10. Simultaneously with the setting of the Write Clock Control FF, the Write Reset FF is reset. The WRS Signal at pin 5 will switch to a logic "0" disabling gate MC94D on the MAG TAPE 1 card. This results in a reset level being applied to the spacing counters. The false WRS signal also disables Write Timing Control at MC86D, and removes the Write Reset level applied to the tape unit through pin 19 allowing the write circuitry to change states depending on the data being written. At the same time that the Write Reset FF on the MAG TAPE 2 card was reset, a Set Flag Buffer signal was generated at MC12 and transmitted to the MAG TAPE 1 card through pin J of the 48 pin connector, where it clocks the Data Flag Buffer FF (MC24B) to the set state due to the fact that the Data Transfer FF is set. At the next computer time period 2, the Data Flag FF (MC35B) will become set, indicating to the software that the interface is now ready to accept the first character of data. If an End-of-Operation interrupt is desired, the program must execute a Set Control operation to the Command Channel. Each time a data character is output to the Data Channel the Data Channel Flag FF must be cleared. The data character is gated into Write Register 1 which consists of MC28A and B, MC37A and B, MC38A and B, and MC57A and B. While the data is in Write Register 1, it is applied to the vertical parity generation network consisting of MC15A and B, and MC16A and B. It is also applied to the Cyclic Redundancy Check Character adder circuitry consisting of MC26A and B, MC36A and B, MC46A and B, MC56A and B, and MC66A. When the next Clock Control Pulse is generated, Write Register 1 is gated to Write Register 2 (MC27A, B, C, and D) and the data is gated to the tape unit. The CRCC adders are clocked into the CRCC Register. The Write Clock signal to the tape unit switches to a logic "0" and a set Flag Buffer signal is generated and transmitted to the MAG TAPE 1 card through pin J. The SFB signal will set the Data Flag Buffer FF and at computer time period 2, the Data Flag FF will become set, again indicating to the software that the interface is ready to accept another data character. Once the last data character has been transmitted, it must be immediately followed by a

Clear Control instruction to the Data Channel. This will cause the Data Transfer FF (MC22B) on the MAG TAPE 1 card to be reset, indicating the end of the transmission of data. When the next Clock Control Pulse occurs, the Write Clock Control FF (MC32) on the MAG TAPE 2 card becomes reset. This inhibits Write Clock timing to the tape unit through gates MC23C, MC23D and Transistor Q10. With the Write Clock Control FF reset and the Write Reset FF reset, the reset input to the CMC divide-by-8 counter (MC22) is removed, allowing it to begin counting Clock Control Pulses. After two Clock Control Pulses have been counted, the Cyclic Redundancy Character FF (MC52) becomes set allowing the contents of the Cyclic Redundancy Check Character Register to be gated to the data lines. During this transfer all bits of the CRCC are inverted except bits 3 and 5. When the CMC Counter (MC22) has counted 3 Clock Control Pulses, NAND gate MC11A outputs a logic "0" which is inverted through gate MC18B and the output clocks Write Register 1 into Write Register 2. Write Register 1 is reset by the output of MC11A. Therefore, both Write Registers are reset to the "0" state. Write Clock timing is again enabled through gates MC43A, MC23C, MC23D, and Transistor Q10. This allows a Write Clock to be generated in order to write the CRCC on the tape. When the fourth Clock Control Pulse has been counted Write Clock timing is again disabled. When the eighth Clock Control Pulse has been counted, the Write Reset FF will be set. The WRS Signal at pin 5 of the MAG TAPE 2 card is applied to pin 5 of the MAG TAPE 1 card. This true WRS signal will turn off Q3 allowing the Write Reset level to be applied to the tape unit. This will switch all write circuitry in the tape unit to the "0" state, at which time the Longitudinal Redundancy Check Character will be written. The true WRS signal is ANDed together with a true WRT at MC94D. The output of this gate is inverted twice through MC94F and MC104. The output of MC104 is ANDed with the set output of the Forward FF at MC94B. The output of MC94B is inverted by MC94C. This will remove the reset level that had been applied to the Spacing Counters. When the pin 8 output of the divide-by-2 counter (MC93B, C and D) becomes true, NAND gate MC95B will be made and the output will switch to the "0" state. The output of this gate is labeled $\overline{\text{SAW}}$, Stop After Write NOT. This level is inverted through MC105B and provides a reset input to the Reverse, Forward and Delay FF's. Upon generation of the next Clock Control Pulse the Forward FF (MC115A) will be reset, removing the Forward Drive signal from the tape unit. Tape motion will stop within 2 milliseconds. At the same time the Delay FF (MC96B) is reset. When this occurs, the reset input to the divide-by-16 counter (MC112) is removed and it begins counting spacing Clock Pulses. After 16 spacing Clock Pulses have been counted, flip-flop MC96A will become set. After an additional 9 spacing Clock Pulses have been counted, NAND gate MC86A will be "made" and the output will switch to a logic "0". This logic "0" will be applied to the direct set input of the Ready FF (MC22A). It is also inverted by NAND gate MC76D, the output of which is labeled SRP (Stop Reset Pulse). The Stop Reset Pulse is applied to the set input of the Delay FF (MC96B). It is also applied to MC72A where it is buffered and inverted by MC72C. The output of MC72C resets the Write FF (MC84A) and directly sets the Read Reset FF (MC115B). Setting of the Read Reset FF will cause Q1 to turn off and a negative true Read Reset level will be applied to the tape unit. This will cause the read circuitry in the tape unit to be held in the "0" state. The clearing of the Write FF will cause NAND gate MC94D to be disabled, thereby restoring the reset input to the spacing counters. The Delay FF (MC96B) will be set when the next Clock Control Pulse is generated. The SRP level from MC76D is applied as a clock input to the Command Flag Buffer FF (MC24A). The set input to this flip-flop is tied to +4.5 volts, therefore, it will switch to the set state. At the next computer time period 2, the ENF signal is generated and the Command Flag FF (MC45C) is set. If the End-of-Operation interrupt feature has been selected the Command Control FF (MC33B) will have been set by program control. If the interrupt system is enabled and the magnetic tape interface has the highest priority on the interrupt chain, at computer time period 5, the SIR level becomes true and NAND gate MC25 is "made" causing the output to switch to a logic "0". This logic "0" input to the Command Interrupt FF (MC26C) will cause it to set. Once this flip-flop becomes set, the necessary Flag and IRQ signals are generated and transmitted to the I/O Address card. The computer will then enter an interrupt sequence.

6-73. It was previously mentioned that the Data Channel flag should be cleared each time a data character is output from the computer. If this sequence is not followed, the Timing FF (MC43) will become set and provide a Timing Error status indication to the computer. The same holds true during a Read operation.

6-74. THE READ OPERATION. To initiate the Read operation a Read command word is transmitted to the Command Channel. This command word is an octal 23. This means that the Motion bit, the Forward bit, and the Data Transfer bit are set to a logic "1". All other bits are "0". Here again, as in the Write operation, a check is made to see if the unit is in the LOCAL mode. If so, the command is rejected. Also a check is made to see if the interface is ready to accept a new command. If not, then the command is rejected. If the unit is in the AUTO mode and the interface is ready to accept a new command, a Motion level is generated, as in the Write operation, at MC54D on the MAT TAPE 1 card. This MOT level is ANDed together with the Forward bit (bit 1) and sets the Forward FF (MC115A). With the Forward FF set Q5 will turn off and a Forward Drive level is transmitted to the magnetic tape unit. The same signal that set the Forward FF is applied to pin 6 of MC75. This results in the generation of the SRS (Start Reset) signal. The Start Reset pulse, which is 200 nanoseconds wide, resets the majority of control flip-flops in the interface circuitry. If the tape is positioned at Load Point, the 3" Gap Control FF (MC116A) will be set. This will cause the tape to be moved forward 3-1/2 inches before any attempt is made to detect the presence of data on the tape. If the tape is

not positioned at Load Point, the 3" Gap Control FF is cleared directly at pin 3. The reset output of the 3" Gap Control FF is ANDed together with an A2 pulse from the frequency dividers. This will cause the Read Reset FF to be reset upon generation of the next Clock Control Pulse. With the Read Reset FF (MC115B) in the reset state, the Read Reset level at pin T of the 48 pin connector is removed. This allows the read circuitry in the tape unit to now attempt to detect the presence of data on the tape. As tape is moved past the read head, the detection of the first data bit will cause the magnetic tape unit to generate a Read Clock. This is a positive false signal and is transmitted to the MAG TAPE 2 card through the 48 pin connector (pin 22). As the pulse is received at the MAG TAPE 2 card, it is delayed 8 microseconds by the circuitry consisting of Q11, C1 and R43. The pulse is then narrowed and applied to the NAND gate, MC105. The output of the NAND gate is labeled RCD (Read Clock Delayed). The Read Data is received at the MAG TAPE 2 card as positive false signals. It is applied to the Longitudinal Redundancy Check Character Register which is made up of MC75A and B, MC76A and B, MC85A and B, MC95A and B, and MC102B. It is also applied to the Read Data Register which is made up of MC86A, B, C, and D, and MC96A, B, C and D. At the same time the data is applied to the vertical parity circuitry which consists of MC83A and B, and MC93A and B. The End-of-Record Control circuitry consisting of Q15, Q16, and MC52B is disabled. The purpose of this circuitry is to detect the absence of two consecutive Read Clocks. Being that a Read Clock signal has been received, this End-of-Record Control circuitry is disabled through MC103C. The Read Clock Delayed signal also steps the divide-by-16 counter (MC63) and generates a Set Flag Buffer signal at MC12C. This Set Flag Buffer signal will be transmitted to the MAG TAPE 1 card through pin J of the 48 pin connector where it will set the Data Flag Buffer FF (MC24B). At the next computer time period 2, the Data Flag FF is set indicating to the computer that the data character is in the buffer register. The data character received is checked for vertical parity, which should always be odd. If a vertical parity error is detected, the PTY FF (MC82) will be set on the trailing edge of the current RCD pulse. If the first data character within a record consists of an octal 23, then it is possible that the record being read is a File Mark record. If this is a File Mark record, then the next two consecutive frames will be blank causing the End-of-Record Control FF to become set. If the next two frames are not blank, then this is a normal data character and will be treated as such. When the next Read Clock is received, again it is delayed and narrowed and the next data character is handled in the same manner as the first. If two consecutive blank frames are read, then the End-of-Record Control FF becomes set. If less than 12 data characters have been read prior to the time that the two blanks are detected, then this is an illegal record length, and parity errors will be generated erroneously and more than one record of data will be read. If 12 or more characters have been read, then the ERC FF (MC52B) becomes set, vertical parity checks are inhibited along with the generation of the SFB signal from MC12C. The setting of the ERC FF enables the divide-by-10 counter (MC53). After seven Clock Control Pulses have been counted it is possible to set the End-of-File FF (MC62B) if this is truly an End-of-File record. In any case, a longitudinal parity check is made. If an error exists, the PTY FF (MC82) becomes set. This will enable the Parity Error status bit on the Command Channel. The End-of-Record FF (MC65B) is set. This causes the ERC FF to reset on generation of the next Clock Control Pulse. When the ERC FF resets the divide-by-10 counter is reset and the Parity Control FF (MC103B) is also reset. The set output of the EOR FF (MC65B) is transmitted to the MAG TAPE 1 card through the 48 pin connector pin 10. The EOR level coming into the MAG TAPE 1 card is ANDed together with a $\overline{\text{WRT}}$ level at MC42E. The output of MC42F directly clears the Data Transfer FF (MC22B). The EOR level is also ANDed with a $\overline{\text{WRT}}$ level at MC94E. The output of MC104 pin 3 is then ANDed with a Forward level and the output of MC94C removes the reset from the spacing counters. When the first Spacing Clock Pulse is generated, MC105A will output a logic "0". The output of MC105A is labeled $\overline{\text{SAR}}$ (Stop After Read NOT). This "0" level is inverted by MC105B and the output provides a reset input to the Forward, Reverse and Delay FF's. On generation of the next Clock Control Pulse the Forward and the Delay FF's will be reset. By resetting the Forward FF, the Forward Drive level to the magnetic tape unit is removed and tape motion will stop within two milliseconds. When the Delay FF (MC96B) was reset, the reset level to the divide-by-16 counter was removed. This allows it to begin counting Spacing Clock Pulses. After 16 SCP's have been counted, MC96A becomes set. After nine more SCP's have been counted NAND gate MC86A outputs a logic "0" which will directly set the Ready FF. The output of MC76D is a logic "1" which is labeled SRP, Stop Reset Pulse. This provides a set input to the Delay FF which will be clocked to the set state on the trailing edge of the next Clock Control Pulse. The SRP level is applied through MC72A inverted by MC72C, the output of which directly sets the Read Reset FF. With the Read Reset FF set, the Read Reset level at pin T of the 48 pin connector will cause the read circuitry in the magnetic tape unit to be disabled. The SRP Signal serves as a clock input to the Command Flag Buffer FF (MC24A) causing it to set. The set output of MC24A is ANDed with the ENF signal and sets the Command Flag FF (MC45C) at the next computer time period 2. If the Command Control FF (MC33B) has been set by program control, the magnetic tape interface card has the highest priority on the interrupt chain, and the interrupt system is enabled, then upon receipt of the SIR signal at the computer time period 5, the output of MC25 will set the Control Interrupt FF (MC26C). This will allow the generation of the appropriate IRQ and Flag Signals to the I/O Address card and the interrupt sequence will be entered.

6-75. A complete timing chart of a Read Operation for a 12 character record has been provided. A careful study of this timing chart will show that the RRC FF (Read

Record Control) on the MAT TAPE 2 card may be set and reset until 12 consecutive data characters have been read. After the 12th data character is read, the RRC FF remains in the reset state. Up until this time it is therefore possible to disable the End-of-Record Control circuitry. This is why a data record must contain a minimum of 12 data characters. It should be noted that during a Write operation a Cyclic Redundancy Check Character was generated and written on the tape 4 frames after the last data character was written. During a Read operation, the Cyclic Redundancy Check Character is completely ignored by the interface. The only reason the Cyclic Redundancy Check Character is generated is in order to make the tape compatible with IBM standards.

6-76. The two major functions of the magnetic tape unit interface have been covered in detail. All other functions are derivations of these. To analyze any secondary functions, utilize the flow charts provided in Section 7.

magnetic tape interface diagrams

SECTION VII
MAGNETIC TAPE INTERFACE DIAGRAMS

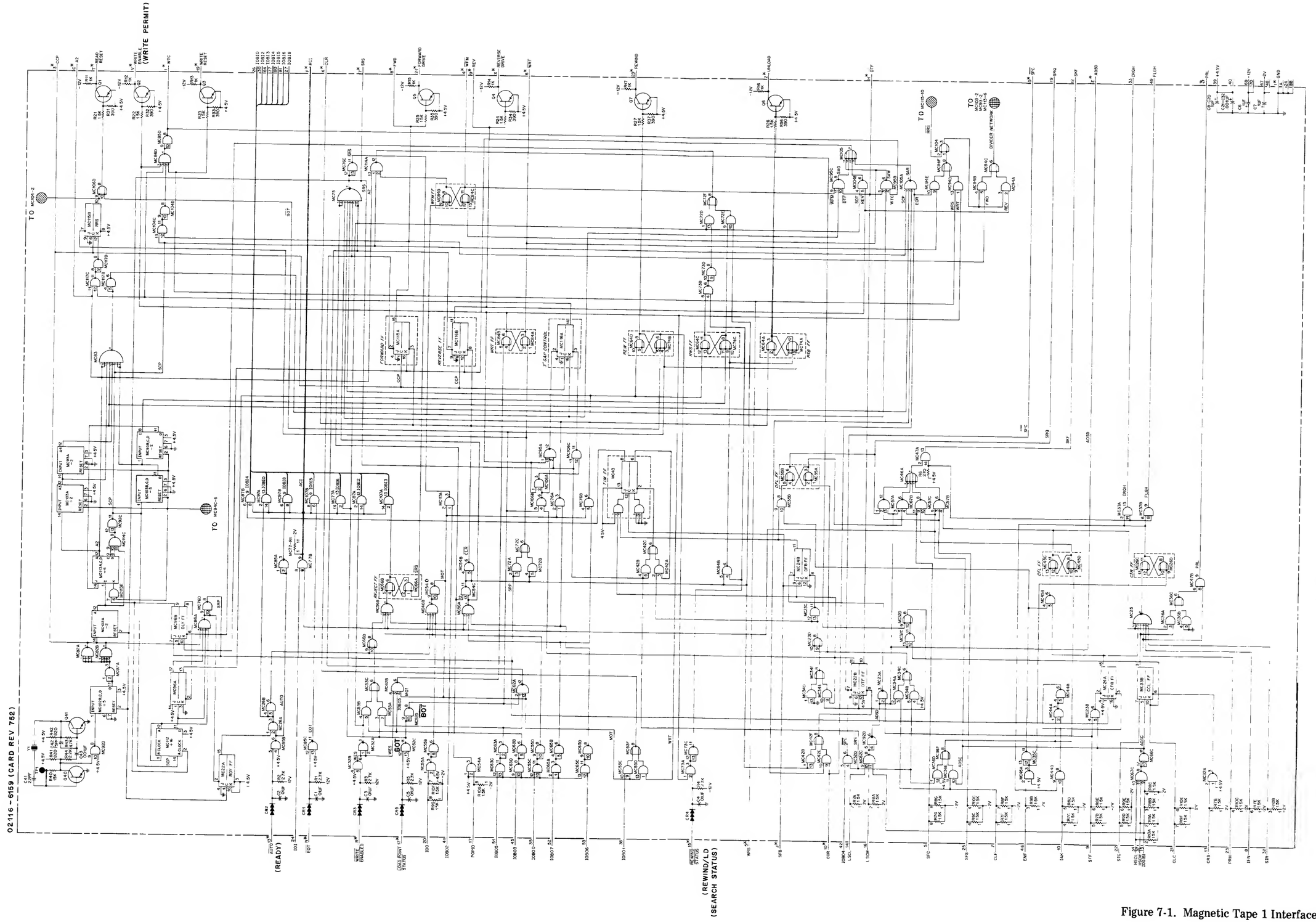
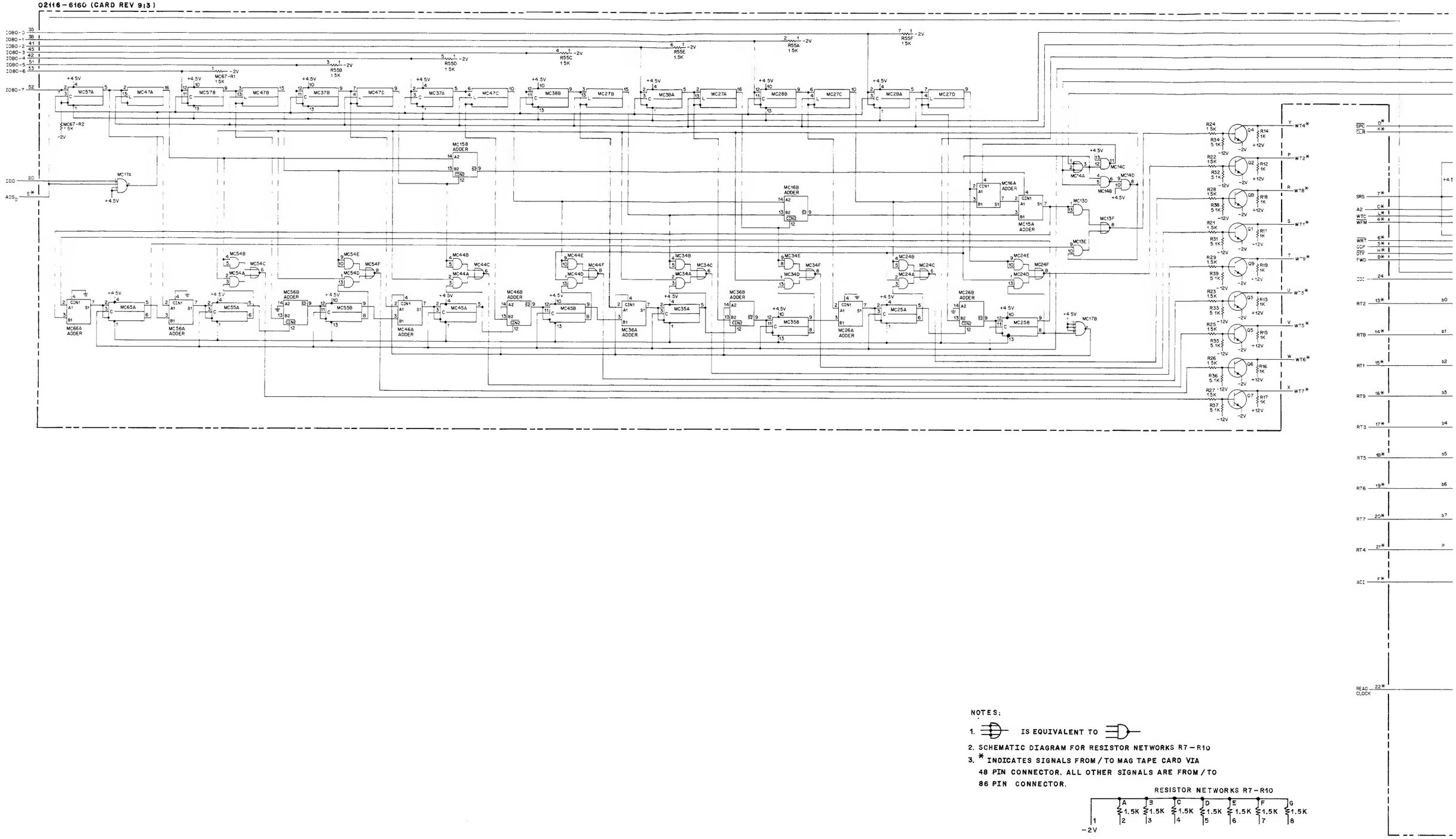


Figure 7-1. Magnetic Tape 1 Interface Card Logic Diagram

02116-6160 (CARD REV 913)



NOTES:

1. IS EQUIVALENT TO
2. SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R7 – R10
3. * INDICATES SIGNALS FROM / TO MAG TAPE CARD VIA 48 PIN CONNECTOR. ALL OTHER SIGNALS ARE FROM / TO 86 PIN CONNECTOR.

RESISTOR NETWORKS R7 – R10

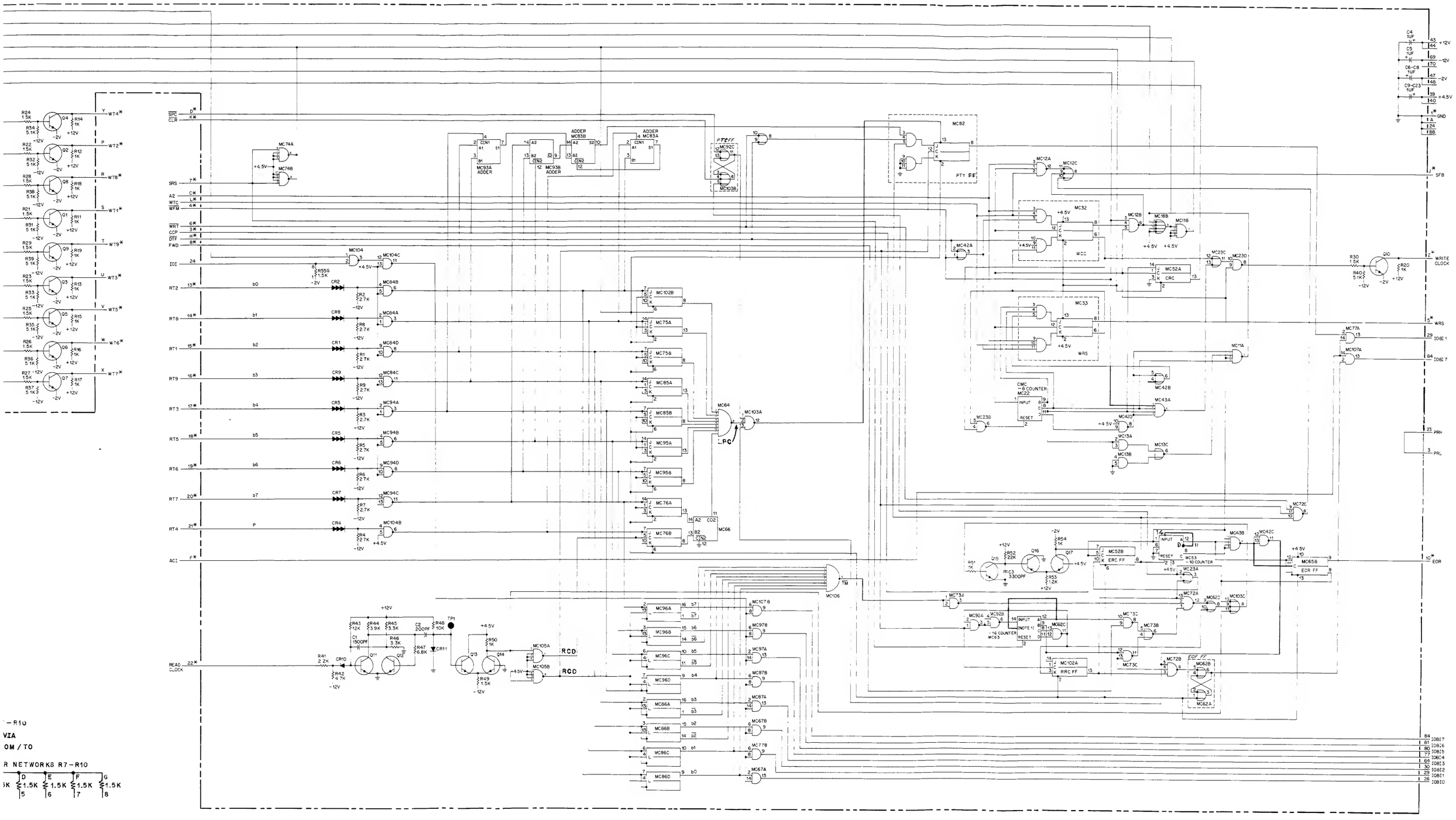


Figure 7-2. Magnetic Tape 2 Interface Card Logic Diagram

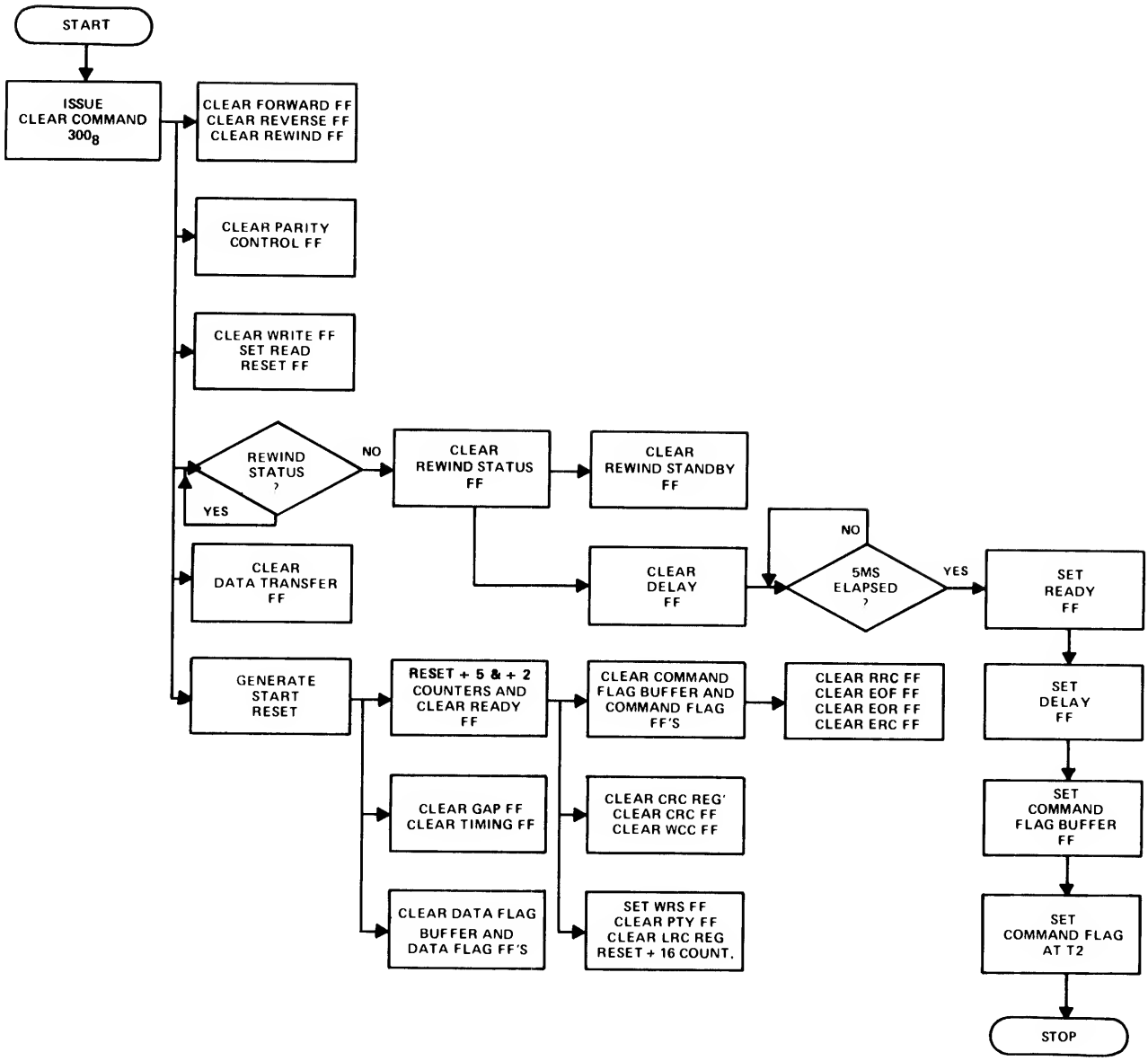
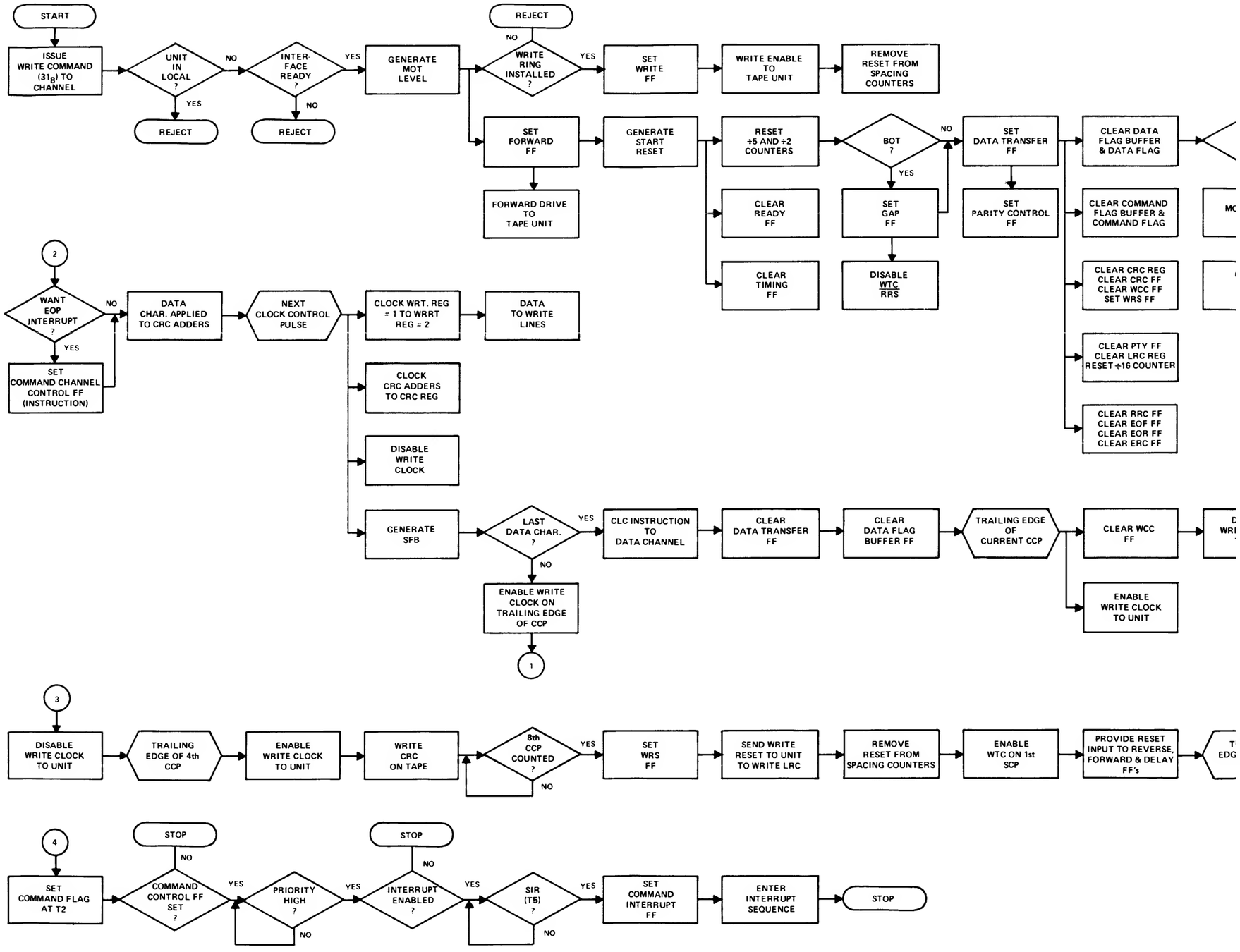


Figure 7-3. Clear Command Flow Chart


START
ISSUE WRITE COMMAND (31_8) TO CHANNEL
UNIT IN LOCAL ?
NO
YES
REJECT
INTER-FACE READY ?
YES
NO
REJECT
GENERATE MOT LEVEL
REJECT
NO
WRITE RING INSTALLED ?
YES
SET WRITE FF
WRITE ENABLE TO TAPE UNIT
REMOVE RESET FROM SPACING COUNTERS
SET FORWARD FF
FORWARD DRIVE TO TAPE UNIT
GENERATE START RESET
RESET ÷5 AND ÷2 COUNTERS
CLEAR READY FF
CLEAR TIMING FF
BOT ?
NO
YES
SET GAP FF
DISABLE WTC RRS
SET DATA TRANSFER FF
SET PARITY CONTROL FF
CLEAR DATA FLAG BUFFER & DATA FLAG
CLEAR COMMAND FLAG BUFFER & COMMAND FLAG
CLEAR CRC REG
CLEAR CRC FF
CLEAR WCC FF
SET WRS FF
CLEAR PTY FF
CLEAR LRC REG
RESET ÷16 COUNTER
CLEAR RRC FF
CLEAR EOF FF
CLEAR EOR FF
CLEAR ERC FF
2
WANT EOP INTERRUPT ?
NO
YES
SET COMMAND CHANNEL CONTROL FF (INSTRUCTION)
DATA CHAR. APPLIED TO CRC ADDERS
NEXT CLOCK CONTROL PULSE
CLOCK WRT. REG = 1 TO WRRT REG = 2
DATA TO WRITE LINES
CLOCK CRC ADDERS TO CRC REG
DISABLE WRITE CLOCK
GENERATE SFB
LAST DATA CHAR. ?
YES
NO
CLC INSTRUCTION TO DATA CHANNEL
CLEAR DATA TRANSFER FF
CLEAR DATA FLAG BUFFER FF
TRAILING EDGE OF CURRENT CCP
CLEAR WCC FF
ENABLE WRITE CLOCK TO UNIT
ENABLE WRITE CLOCK ON TRAILING EDGE OF CCP
1
3
DISABLE WRITE CLOCK TO UNIT
TRAILING EDGE OF 4th CCP
ENABLE WRITE CLOCK TO UNIT
WRITE CRC ON TAPE
8th CCP COUNTED ?
YES
NO
SET WRS FF
SEND WRITE RESET TO UNIT TO WRITE LRC
REMOVE RESET FROM SPACING COUNTERS
ENABLE WTC ON 1st SCP
PROVIDE RESET INPUT TO REVERSE, FORWARD & DELAY FF's
4
SET COMMAND FLAG AT T2
STOP
NO
COMMAND CONTROL FF SET ?
YES
PRIORITY HIGH ?
YES
NO
STOP
NO
INTERRUPT ENABLED ?
YES
SIR (T5) ?
YES
NO
SET COMMAND INTERRUPT FF
ENTER INTERRUPT SEQUENCE
STOP

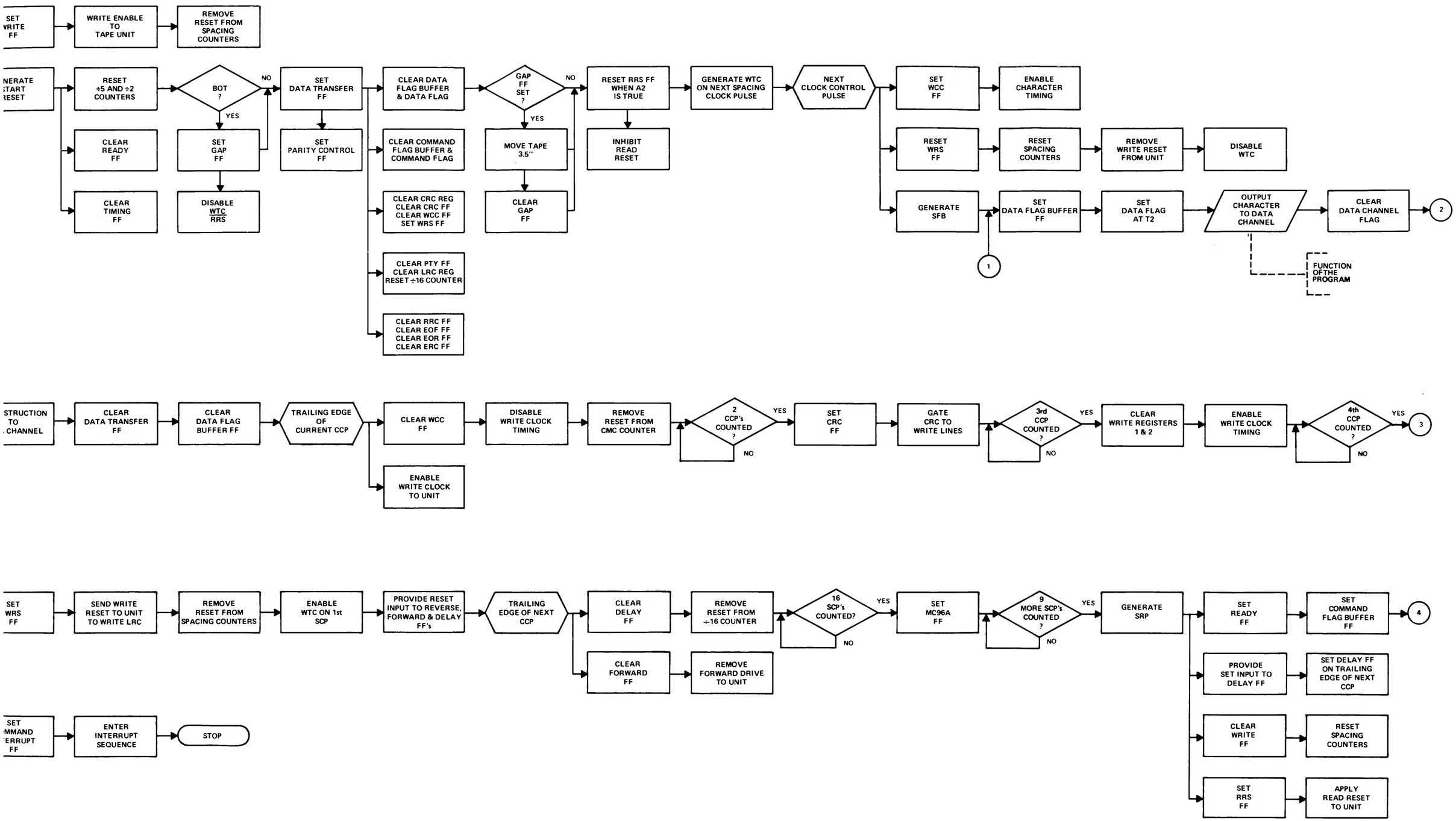


Figure 7-4. Write Operation Flow Chart

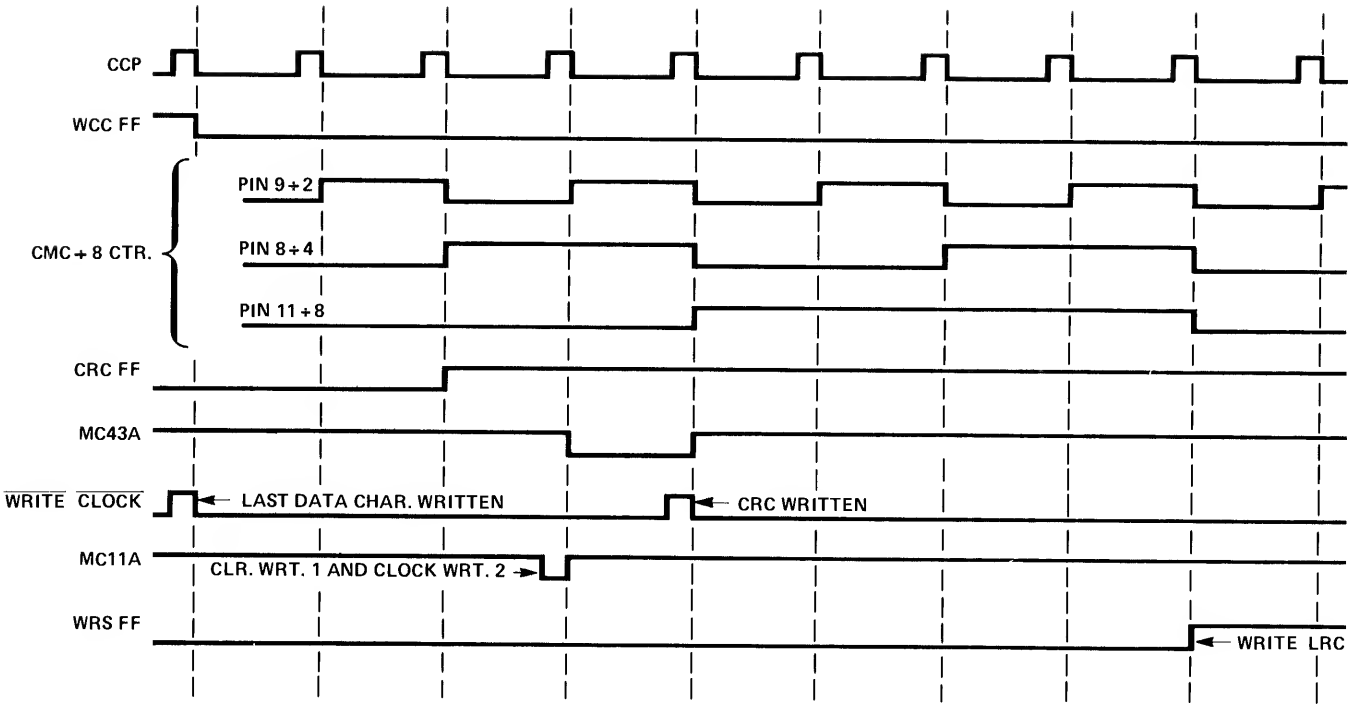


Figure 7-5. End of Write Operation Timing Diagram

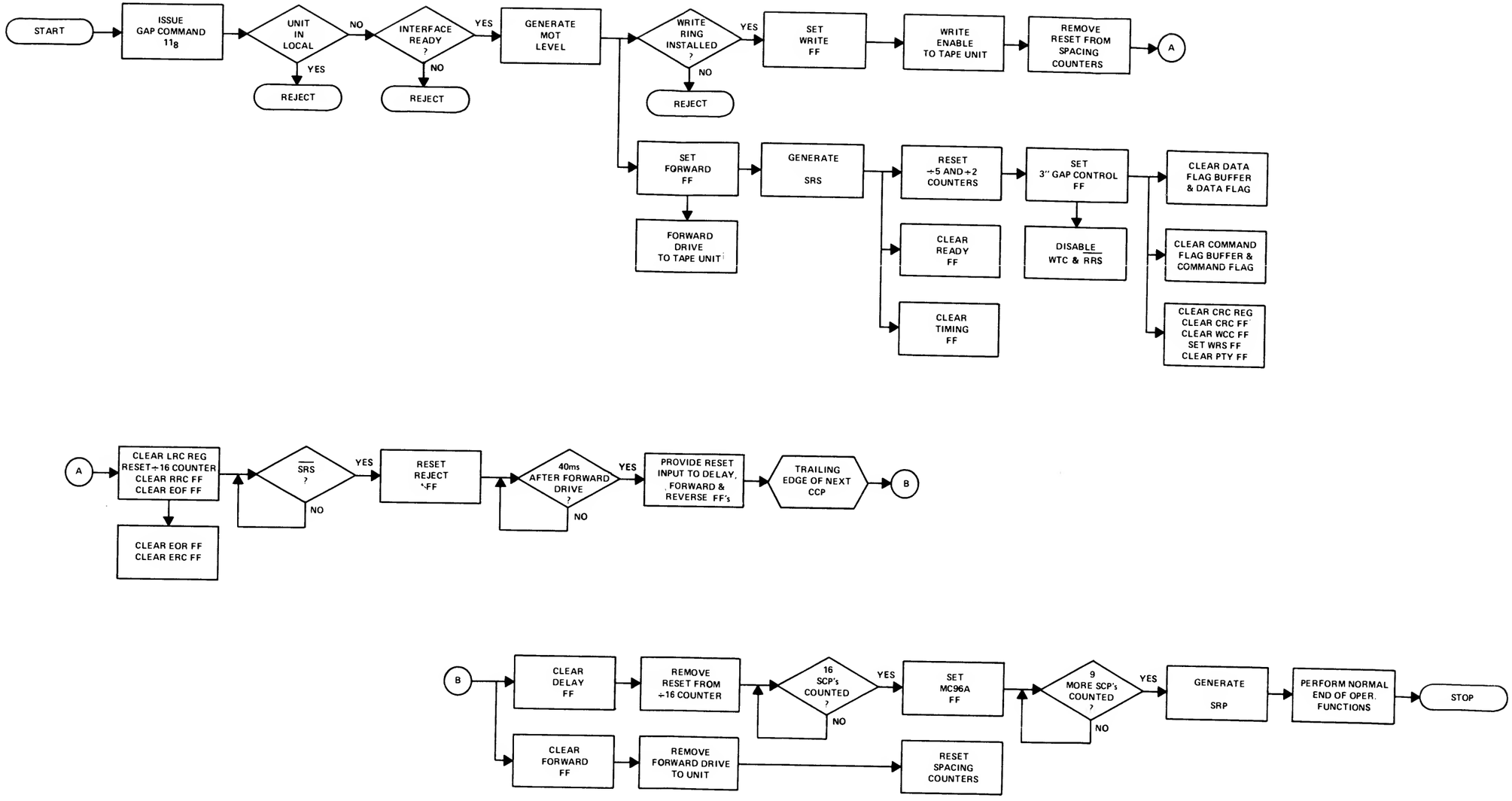
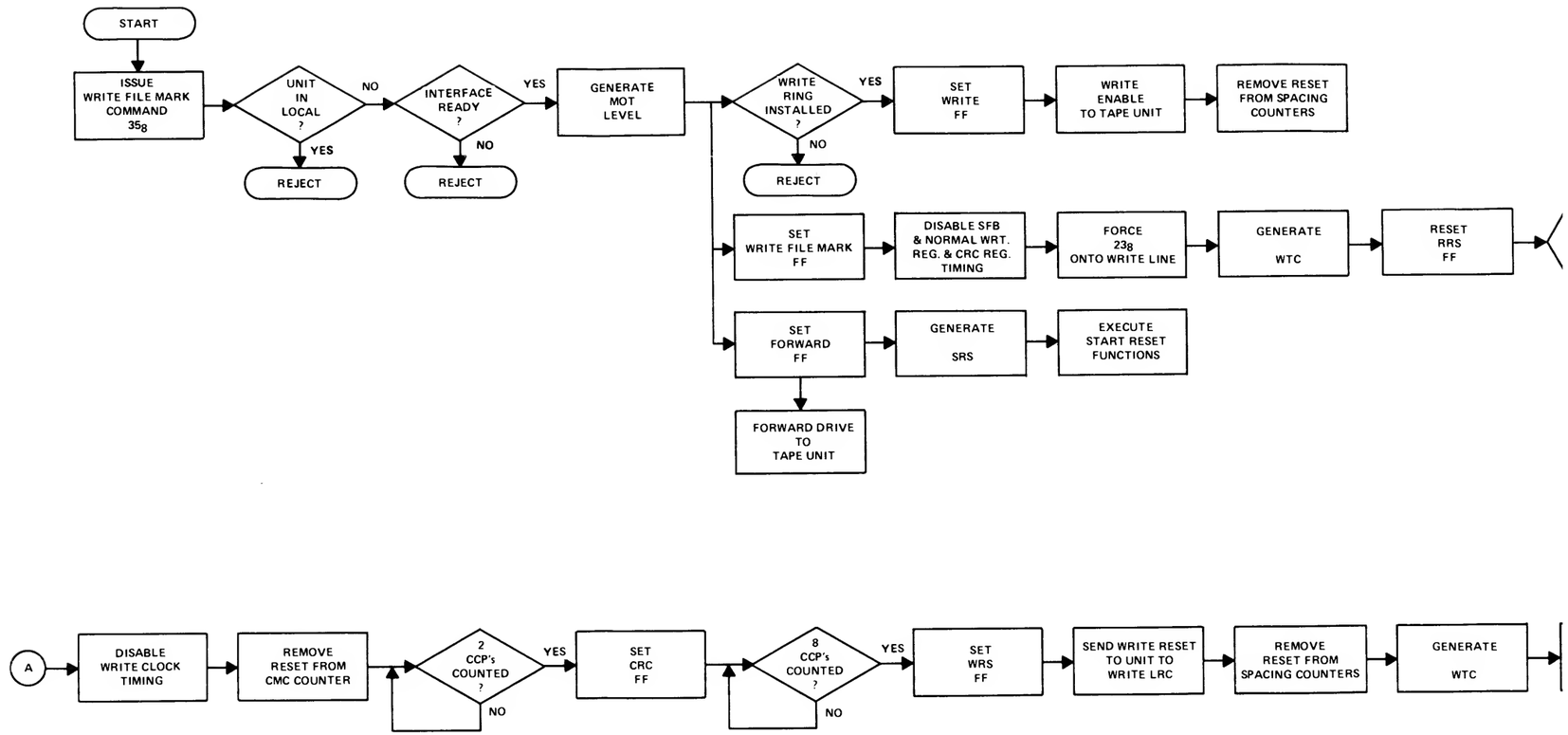


Figure 7-6. Three-inch Gap Operation Flow Chart


START
ISSUE WRITE FILE MARK COMMAND 35_8
UNIT IN LOCAL ?
NO
YES
REJECT
INTERFACE READY ?
YES
NO
REJECT
GENERATE MOT LEVEL
WRITE RING INSTALLED ?
YES
NO
REJECT
SET WRITE FF
WRITE ENABLE TO TAPE UNIT
REMOVE RESET FROM SPACING COUNTERS
SET WRITE FILE MARK FF
DISABLE SFB & NORMAL WRT. REG. & CRC REG. TIMING
FORCE 23_8 ONTO WRITE LINE
GENERATE WTC
RESET RRS FF
SET FORWARD FF
GENERATE SRS
EXECUTE START RESET FUNCTIONS
FORWARD DRIVE TO TAPE UNIT
A
DISABLE WRITE CLOCK TIMING
REMOVE RESET FROM CMC COUNTER
2 CCP's COUNTED ?
YES
NO
SET CRC FF
8 CCP's COUNTED ?
YES
NO
SET WRS FF
SEND WRITE RESET TO UNIT TO WRITE LRC
REMOVE RESET FROM SPACING COUNTERS
GENERATE WTC

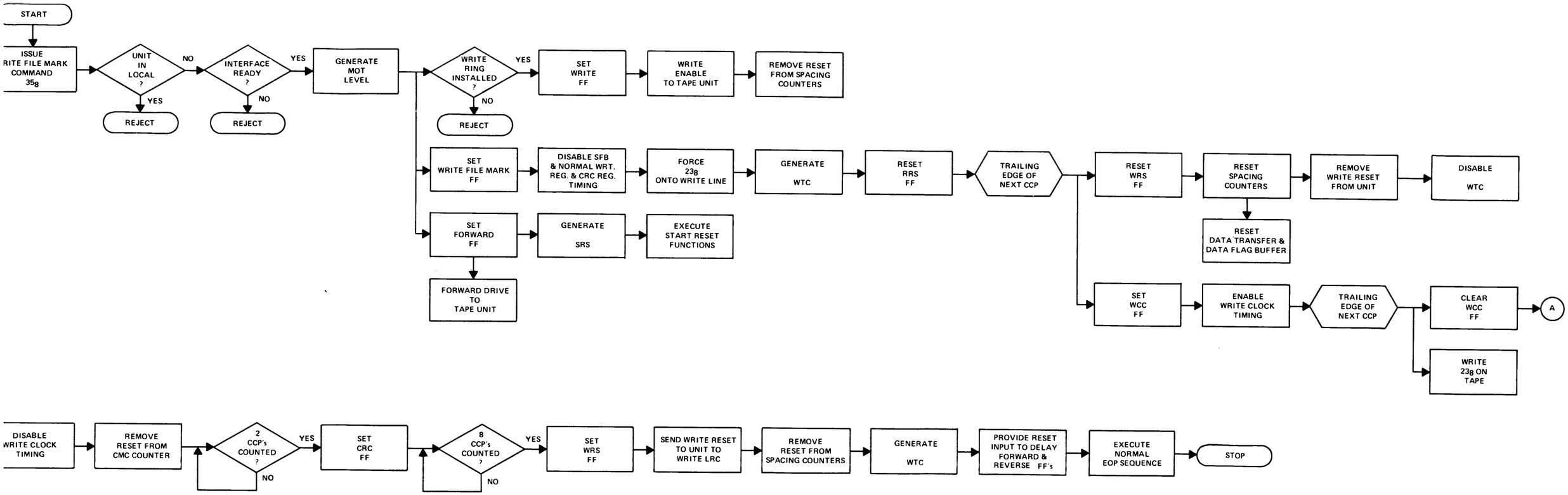
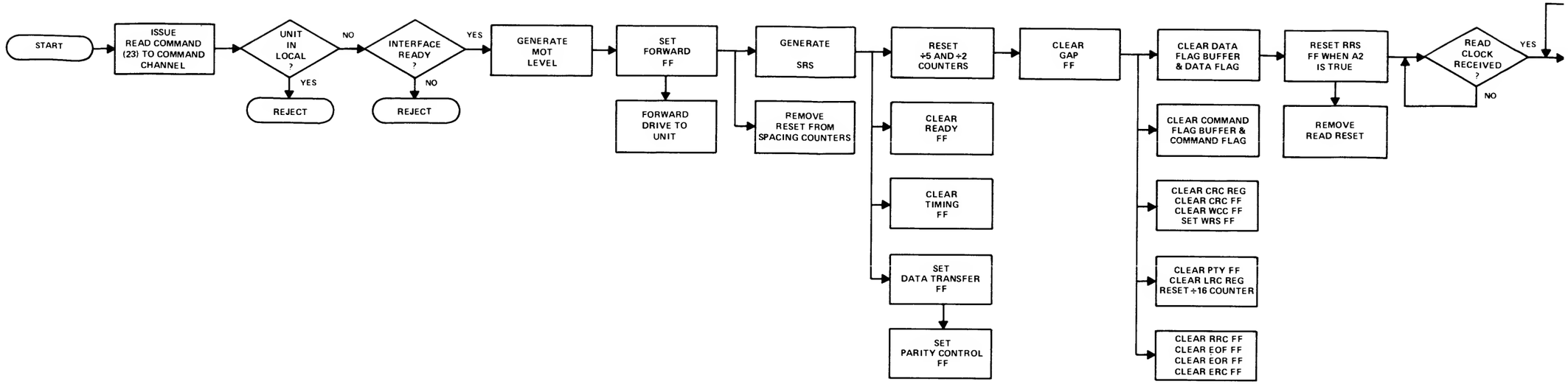


Figure 7-7. Write File Mark Flow Chart


START
ISSUE READ COMMAND (23) TO COMMAND CHANNEL
UNIT IN LOCAL ?
YES
REJECT
NO
INTERFACE READY ?
YES
NO
REJECT
GENERATE MOT LEVEL
SET FORWARD FF
FORWARD DRIVE TO UNIT
GENERATE SRS
REMOVE RESET FROM SPACING COUNTERS
RESET ÷5 AND ÷2 COUNTERS
CLEAR READY FF
CLEAR TIMING FF
SET DATA TRANSFER FF
SET PARITY CONTROL FF
CLEAR GAP FF
CLEAR DATA FLAG BUFFER & DATA FLAG
CLEAR COMMAND FLAG BUFFER & COMMAND FLAG
CLEAR CRC REG
CLEAR CRC FF
CLEAR WCC FF
SET WRS FF
CLEAR PTY FF
CLEAR LRC REG
RESET ÷16 COUNTER
CLEAR RRC FF
CLEAR EOF FF
CLEAR EOR FF
CLEAR ERC FF
RESET RRS FF WHEN A2 IS TRUE
REMOVE READ RESET
READ CLOCK RECEIVED ?
YES
NO
1
2
12 OR MORE CHAR. READ ?
YES
NO
ILLEGAL RECORD LENGTH. FALSE P.E.'s WILL BE GENERATED
STOP
SET ERC FF AFTER TWO BLANK FRAMES
INHIBIT VERTICAL PARITY CHECKS
INHIBIT SFB
ENABLE ÷10 COUNTER
7 CCP's COUNTED
YES
NO
EOF OPERATION ?
YES
NO
SET EOF FF
CHECK FOR LONGITUDINAL PARITY ERROR
SET EOR FF
RESET ERC FF ON NEXT CCP
RESET PTC FF
RESET ÷10 COUNTER
CLEAR DATA TRANSFER FF
DISABLE RESET TO SPACING COUNTERS
SCP & ÷2 (MC93B,C,D) TRUE ?
YES
NO
TRAILING EDGE OF NEXT CCP
3
GENERATE SRP
SET READY FF
SET COMMAND FLAG BUFFER FF
PROVIDE SET INPUT TO DELAY FF
SET DELAY FF ON TRAILING EDGE OF NEXT CCP
SET RRS FF
APPLY READ RESET TO UNIT
SET COMMAND FLAG AT T2
COMMAND CONTROL FF SET ?
YES
NO
STOP
PRIORITY HIGH ?
YES
NO
INTERRUPT ENABLED ?
YES
NO
STOP
SIR ?
YES
NO
SET COMMAND INTERRUPT FF
ENTER INTERRUPT SEQUENCE
STOP

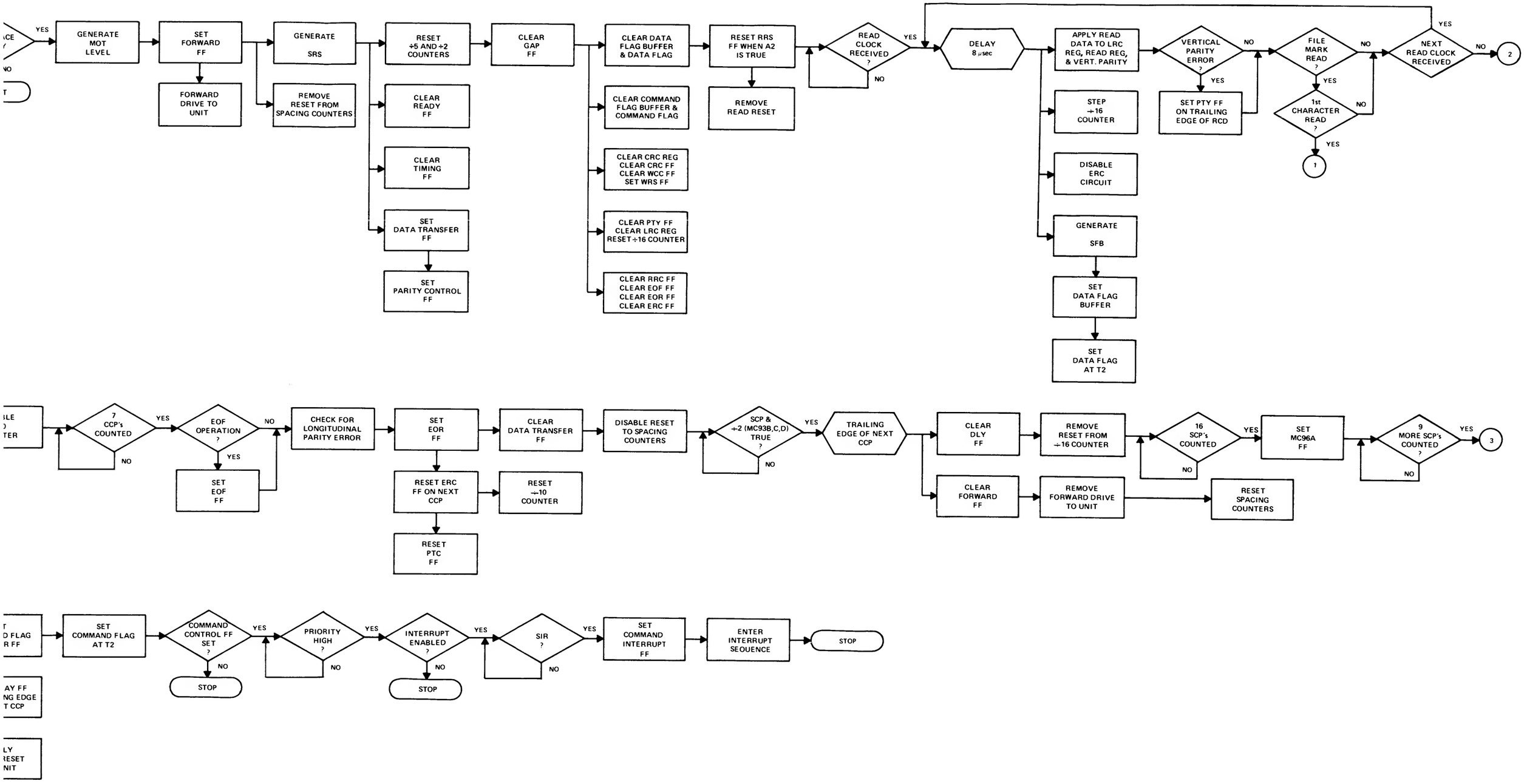
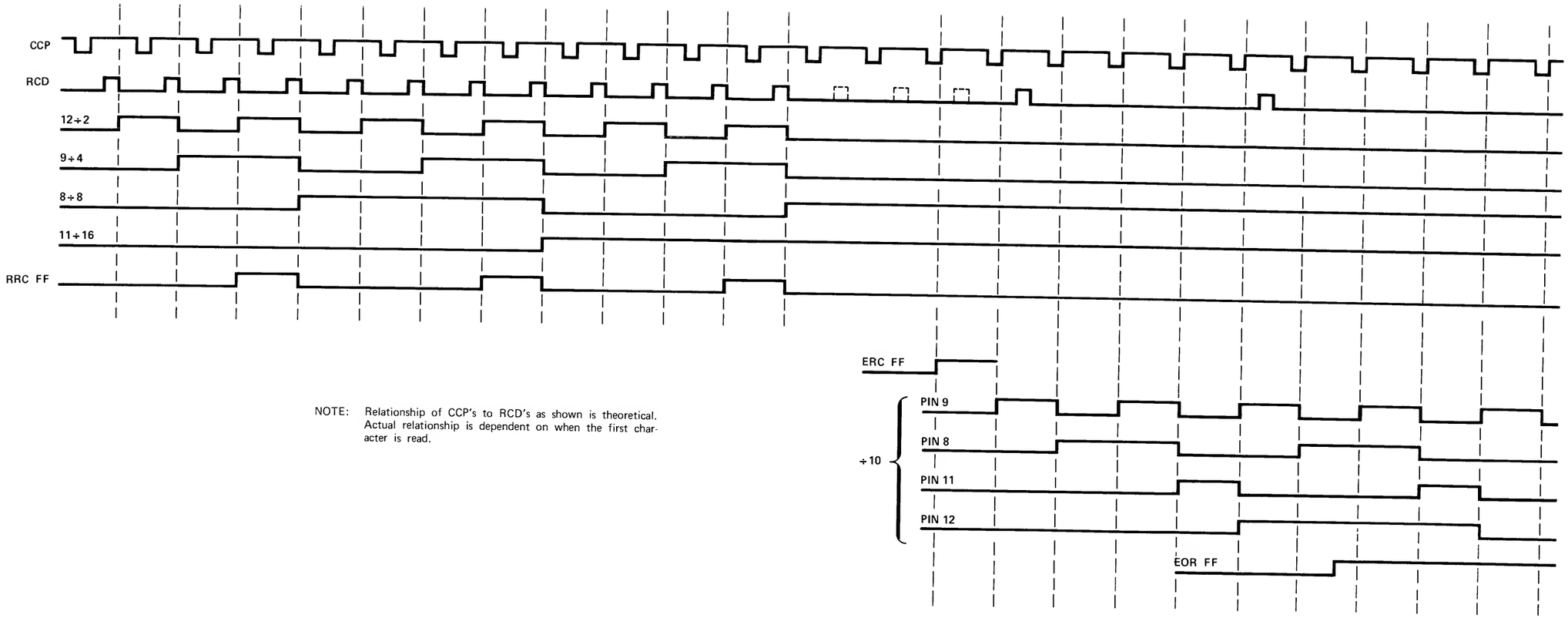


Figure 7-8. Read Operation Flow Chart



NOTE: Relationship of CCP's to RCD's as shown is theoretical. Actual relationship is dependent on when the first character is read.

Figure 7-9. Read Operation of 12 Characters, Timing Diagram

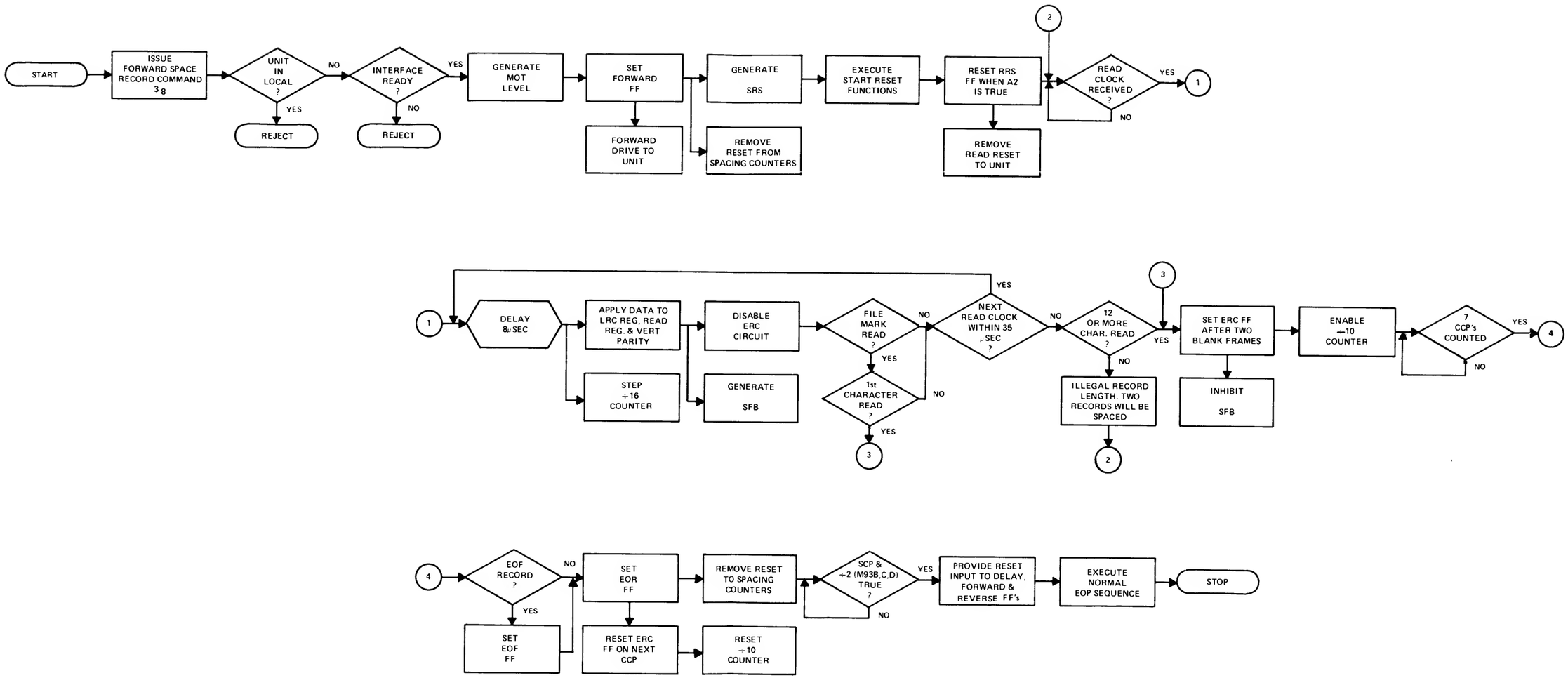
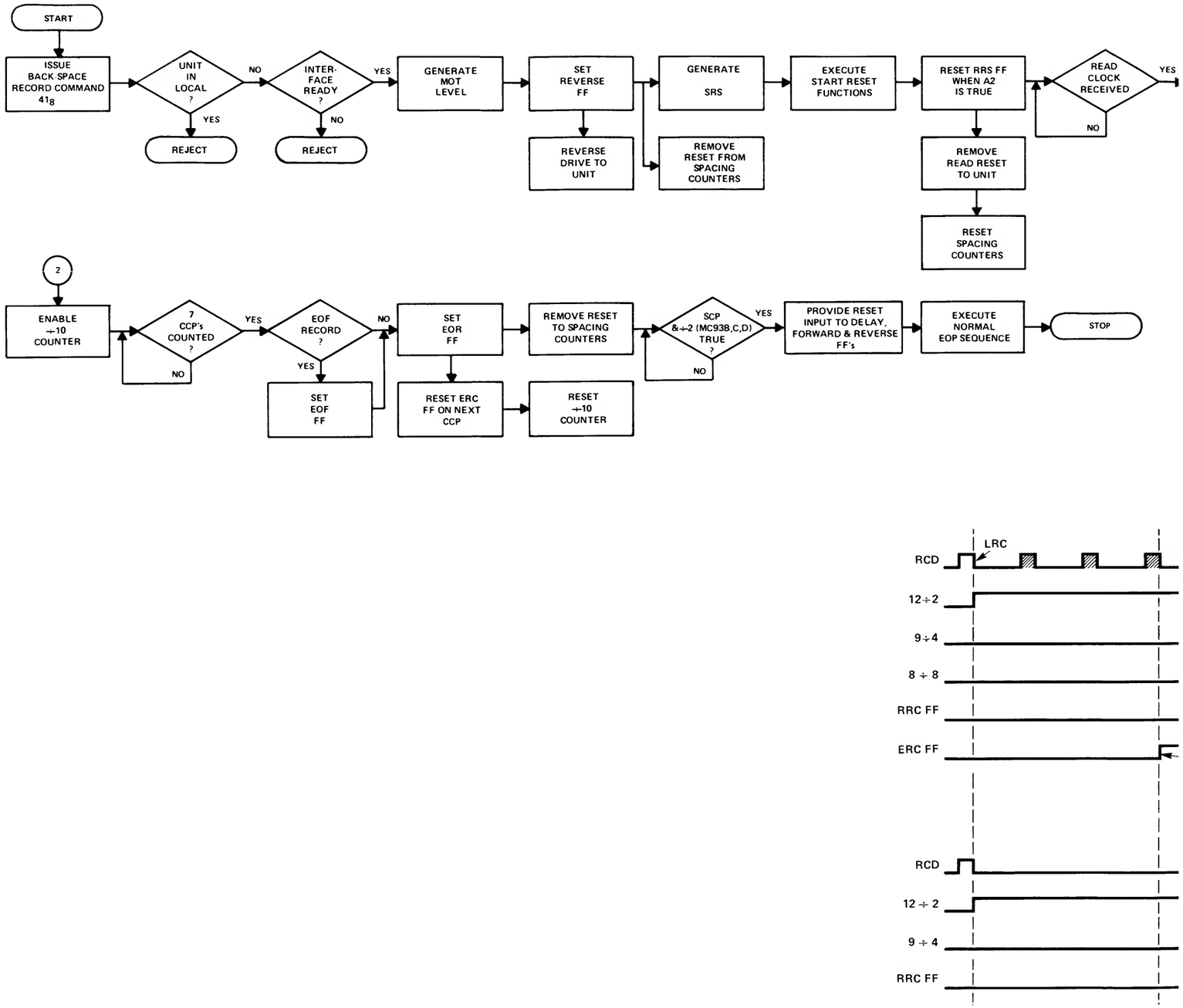


Figure 7-10. Forward Space Record Flow Chart


START
ISSUE BACK SPACE RECORD COMMAND 41_8
UNIT IN LOCAL ?
NO
YES
REJECT
INTER-FACE READY ?
YES
NO
REJECT
GENERATE MOT LEVEL
SET REVERSE FF
REVERSE DRIVE TO UNIT
GENERATE SRS
REMOVE RESET FROM SPACING COUNTERS
EXECUTE START RESET FUNCTIONS
RESET RRS FF WHEN A2 IS TRUE
REMOVE READ RESET TO UNIT
RESET SPACING COUNTERS
READ CLOCK RECEIVED
YES
NO
2
ENABLE ÷10 COUNTER
7 CCP's COUNTED ?
YES
NO
EOF RECORD ?
YES
SET EOF FF
NO
SET EOR FF
RESET ERC FF ON NEXT CCP
REMOVE RESET TO SPACING COUNTERS
RESET ÷10 COUNTER
SCP &÷2 (MC93B,C,D) TRUE ?
YES
NO
PROVIDE RESET INPUT TO DELAY, FORWARD & REVERSE FF's
EXECUTE NORMAL EOP SEQUENCE
STOP

LRC
RCD
12÷2
9÷4
8 ÷ 8
RRC FF
ERC FF
RCD
12 ÷ 2
9 ÷ 4
RRC FF

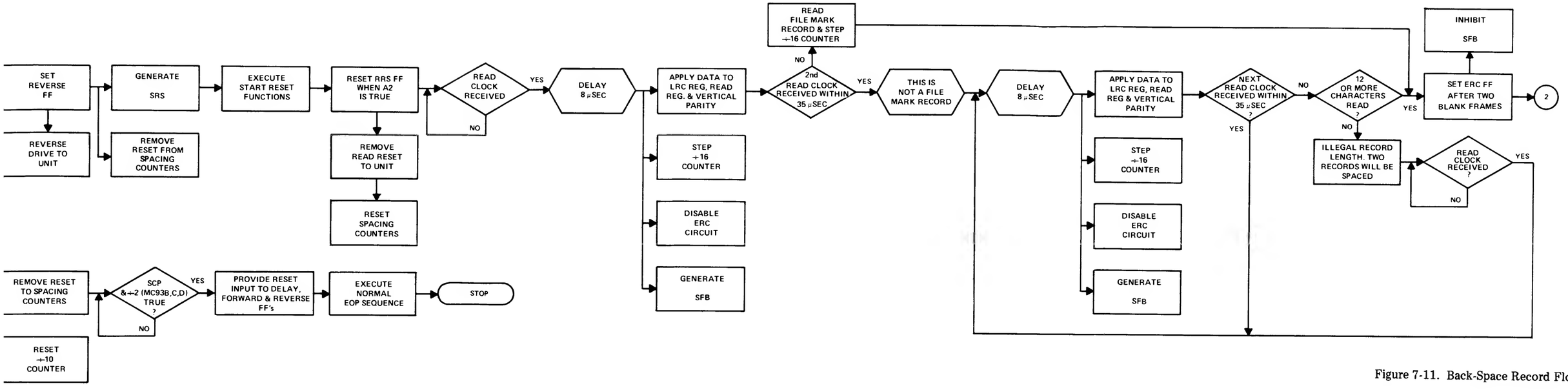


Figure 7-11. Back-Space Record Flow Chart

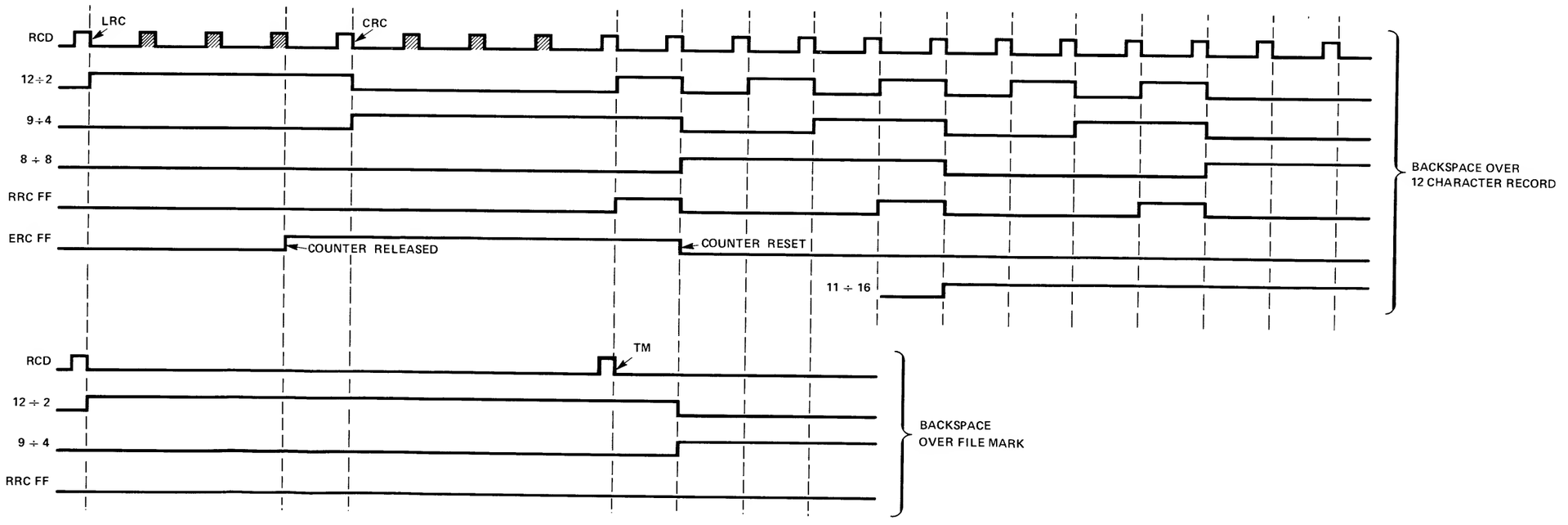


Figure 7-12. Back-space operations Timing Diagram

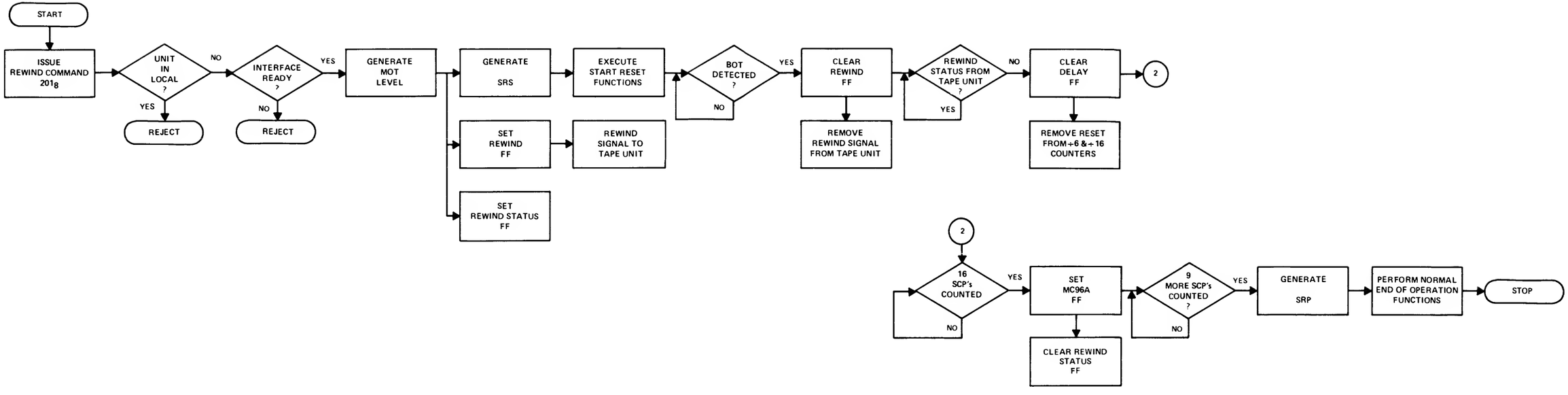


Figure 7-13. Rewind Standby Flow Chart

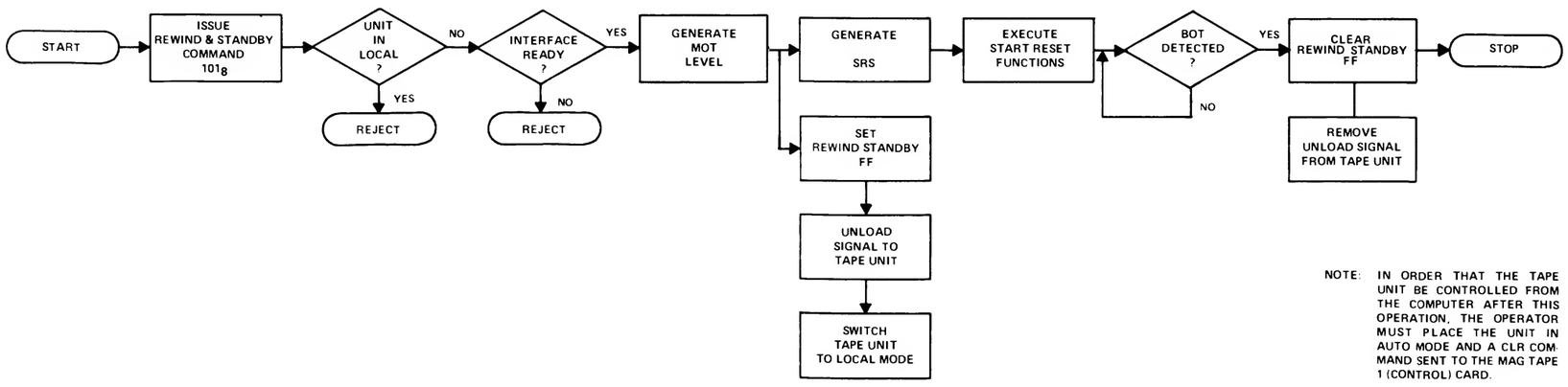


Figure 7-14. Rewind Operation Flow Chart

SECTION VIII

H01-D3030 DIAGNOSTIC PROGRAM 20433E

8-1. 9-TRACK MAGNETIC TAPE.

8-2. This diagnostic program checks the capability of the HP 3030 Magnetic Tape Unit to write and read data correctly with the HP Computer. The program is entered into the Computer by either the Punched Tape Reader or Teleprinter. If an error occurs a diagnostic (code or description) will be printed. Contained on the tape is a main program and four secondary programs. Five additional tests can be added to the main program by manual selection of front panel switches. Secondary programs provide detailed analysis of malfunctions detected by the main program or the five tests added to it.

8-3. MAIN DIAGNOSTIC PROGRAM.

8-4. This program checks the standard operations of the tape unit and interface cards. Refer to Table 8-1, Magnetic Tape Troubleshooting Chart, for the tests performed. Figure 8-1 depicts the test pattern, halt position numbers, and the location within the pattern at which they occur. With all switches of the Switch Register down, the main diagnostic program is continually repeated.

8-5. OPERATING PROCEDURES.

8-6. To initialize the diagnostic program, perform the following:

a. Enter octal 100 into S-Register.

b. Press LOAD ADDRESS.

c. Use S-Register bits 0 through 5 and enter octal address of the I/O slot containing the Mag. Tape 1 board (02116-6159).

d. If a 2.0 μsec Computer is being used, set S-Register bit 15 to 1. If a 1.6 μsec Computer (2116A/B) is being used, set S-Register bit 15 to 0.

e. Push RUN.

f. Use the S-Register bit 0 through 5 and enter the octal address of the I/O slot containing the teleprinter interface card.

g. If a serial teleprinter card is being used, set the S-Register bit 15 to 1. If a buffered teleprinter card is being used, set the S-Register bit 15 to 0.

h. Push RUN.

i. Enter top memory location into S-Register

4K — 07777
8K — 17777
12K — 27777
16K — 37777
24K — 57777
32K — 77777

j. Push RUN.

Note

If an error occurs during the above procedures, reload the diagnostic tape. After the diagnostic tape is loaded into memory, the starting address of the program is 2000.

Table 8-1. Magnetic Tape Troubleshooting Chart

HALT NUMBER	DIAGNOSTIC OPERATION	PROBABLE CAUSE AND/OR REMEDY
1	CLR Command	Clear Command should reset all CONTROL LOGIC 1. If busy, check DLY, RDY, Timing logic. 2. Check individual status FF's.
2-5	Check Computer control of Data Flag	
*2	Clear Data Flag and give SFC data	Either flag not cleared or SFC data instruction does not work.
*3	Give SFS data	If 2 and 3, Data Flag not clear. If 3 only, SFS Data Instruction malfunction.
*4	Set Data Flag and give SFS data	Either flag not set or SFS data instruction malfunction.

*Use Switch 14 as explained in Table 8-2.
Data is mnemonic for higher priority magnetic tape address.
Command is mnemonic for lower priority magnetic tape address.

Table 8-1. Magnetic Tape Troubleshooting Chart (Continued)

HALT NUMBER	DIAGNOSTIC OPERATION	PROBABLE CAUSE AND/OR REMEDY
*5	Give SFC data	If 4 and 5, Data Flag not set. If 5 only, SFS Data instruction malfunction.
6-13	Command Flag and Interrupt check	
6	Turn on INTRPT SET CMND Flag but no Control Bit	Should not interrupt without CCC flip-flop set.
7	STC CMND	Should interrupt. Check if Flag set, Control FF set.
*10	Clear CMND Flag and give SFC	Either flag not cleared of SFC CMND malfunction.
*11	Give SFS CMND	If 10 and 11, flag not clear. If 11 only, SFS CMND malfunction.
*12	Set CMND Flag and give SFS CMND	Either flag not set of SFS CMND malfunction.
*13	Give SFC CMND	If 12 and 13, flag not set. If 13 only, SFC CMND malfunction.
14-17	Check Timing Logic	
14	Give CLR Command after 4.9 msec	A CLR command should set controller busy for 5 msec. RDY either not cleared or set too soon.
15	after 5.1 msec	DLY should count 5 msec and set RDY. Check oscillator, timing circuits, DLY FF and RDY FF.
16	Give GAP Command after 44.9 msec	A GAP command should take 40 msec of spacing +5 msec of RDY. Check GAP FF and timing circuits.
17	after 45.1 msec	Check timing circuits.
20	Check REJ status	If controller is busy (with a CLR command) it should REJ a command from computer. Check REJ FF.
21-26	Initial Data Transfer Check	Write various tracks and read back as data passes under Read Head.
*21	Write all tracks	Either not writing bits or reading them back in erroneous tracks. 1. Is there a write clock? 2. Is WRT set, WRS cleared? 3. Read, write cards in transporter?
*22	Write Track 4	Same as above
*23	Write Tracks 1, 2, 3, 4, and 6	Same as above

*Use Switch 14 as explained in Table 8-2.

Table 8-1. Magnetic Tape Troubleshooting Chart (Continued)

HALT NUMBER	DIAGNOSTIC OPERATION	PROBABLE CAUSE AND/OR REMEDY
*24	Write Tracks 4, 5, 7, 8, and 9	Either not writing bits or reading them back in erroneous tracks. 1. Is there a write clock? 2. Is WRT set, WRS reset? 3. Read, write cards in transporter?
*25	Write Tracks 1, 3, 4, 5, 7, and 9	Same as above
*26	Write Tracks 1, 2, 4, 6, and 8	Same as above
27-45	Write Records for Later Read Checks	
*27	Write All Tracks	Status should be clear after write. 1. If parity error, check parity generation for this bit; parity check for this bit; check longitudinal parity. 2. If other, check individual status.
*30	Write Parity Bit	Same as above
31	Write Bit 0	Same as above
32	Write Bit 1	Same as above
33	Write Bit 2	Same as above
34	Write Bit 3	Same as above
35	Write Bit 4	Same as above
36	Write Bit 5	Same as above
37	Write Bit 7	Same as above
40	Write Bit 8	Same as above
41	Write all Tracks; 12 Character RECORD	Twelve characters is minimum length record. If parity, 1. Check character counter MC63. 2. Check parity circuits. If other, check individual status.
*42	Write CRC Check Record	Eleven data characters should make CRCC vertical parity even-force parity error. If no parity error, check CRCR.
*43	Write Non-Valid File Mark	If FM status, check EOF detection, EOR detection.
*44	Write Checkerboard	All tracks except 2 are alternate 1's and 0's. Check individual status.
*45	Write File Mark	If no FM, check EOR, EOF detection. Check individual status.

*Use Switch 14 as explained in Table 8-2.

Table 8-1. Magnetic Tape Troubleshooting Chart (Continued)

HALT NUMBER	DIAGNOSTIC OPERATION	PROBABLE CAUSE AND/OR REMEDY
46-63	Backspace over records. Initial Read Control Stop of Tape.	
46	Backspace over FM.	If not FM, check EOR, EOF detection on backspace. If SOT, check read clock, EOR detection.
47	Backspace A Record	If SOT, check read block, EOR detection.
50	Backspace A Record	Should not stop on non-valid tape mark record. This will show up by the tape being misplaced at HALT 71.
51	Backspace A Record	If SOT, check read clock, EOR detection.
52	Backspace A Record	Same as above
53	Backspace A Record	Same as above
54	Backspace A Record	Same as above
55	Backspace A Record	Same as above
56	Backspace A Record	Same as above
57	Backspace A Record	Same as above
60	Backspace A Record	Same as above
61	Backspace A Record	Same as above
62	Backspace A Record	Same as above
63	Backspace A Record	Same as above
64	Forward Space over all ones record	Check read clock, EOR detection. Check individual status.
65	Backspace	If SOT, check read clock, EOR detection.
66	Check for CMND INTRPT on READ	If no interrupt, check EOR detection CMND flag and interrupt circuit.
67	Check Status After Read	Check individual status.
70	Backspace A Record	If SOT, check read clock, EOR detection
71-103	Read Data Checks	
71	Read all ones record	If data error check writing circuits reading circuits read clock, write clock If status, check individual status.
72	Read Parity or only record	If data error check writing circuits reading character reading clock, write clock If status, check individual status

Table 8-1. Magnetic Tape Troubleshooting Chart (Continued)

HALT NUMBER	DIAGNOSTIC OPERATION	PROBABLE CAUSE AND/OR REMEDY
73	Read Bit 0 Record	If data error check writing circuits reading character reading clock write clock If status, check individual status.
74	Read Bit 1 Record	Same as above
75	Read Bit 2 Record	Same as above
76	Read Bit 3 Record	Same as above
77	Read Bit 4 Record	Same as above
100	Read Bit 5 Record	Same as above
101	Read Bit 6 Record	Same as above
102	Read Bit 7 Record	Same as above
103	Read 12 Character Record	Same as above
104	FSR Command	Should move over 11 character record. No parity error on FSR. Check individual status.
105	Backspace A Record	If SOT, check read block, EOR detection.
106	Read CRC Record	If data character 12 wrong, check CRCC generation. If no parity error, check parity generation, clock, and CRC generation. If short, check for EOR detection.
107-110	Check Inter-Record GAP Length	Read 2 character non-valid tape mark record. Count the time until data from checkerboard record (past IRG) encountered.
107		Gap too small: 1. tape unit not 75 ips, or 2. T_{SAW} or T_{WAS} too short.
110		Gap too long; either 1. tape unit not 75 ips, or 2. T_{SAW} or T_{WAS} too long,or 3. actuators slipping.
111	Check Status for Forced TM Error	If no TM error, check TIM flip-flop
112	Backspace A Record	If SOT, check read clock, EOR detection.
113	Read Checkerboard Record	Status Should be clear. Data Errors — check write and read circuits. Parity Errors — check parity generate and check. Length Errors — check read clock.
114	Detect EOF on FSR	Check EOR and EOF detection circuits.
115	Detect EOF on BSR	Check EOR and EOF detection circuits.

Table 8-1. Magnetic Tape Troubleshooting Chart (Continued)

HALT NUMBER	DIAGNOSTIC OPERATION	PROBABLE CAUSE AND/OR REMEDY
116	Read EOF	Check write and read electronics.
117-120	Check WAS Time	First flag on write is given 5.2 msec after command.
117	Flag Too Late	Check if Timing circuits working WTC, A_2 generated.
120	Flag Too Early	Check if gates forming WTC work. Check WCC and WRS off.
121-122	Check RAS Time	Write a long record, backspace into it, stop, and then give read command to check RAS time.
121	Data Flag Too Early	Check if RRS set too soon.
122	Data Flag Too Late	Check if RRS not set. Read clock delayed circuit.
123-124	Check SAW Time	Stop a write operation and count when flag returned.
123	SAW Time Short	Check counter circuits.
124	SAW Time Long	Check if WRS clear. Check counter circuits.
125	Backspace A Record	If SOT, check read clock, EOR detection.
126-127	Check SAR Backward; RAS Forward	Having backspaced over record, now read it.
126	Data Flag Too Soon	Check reverse actuator stop time or forward actuator starting time.
127	Data Flag Too Soon	Check reverse actuator stop time or forward actuator start time.
130-131	Check RAS Time	Count time from last data character read to CMND flag returned.
130	SAR Time Short	Check counter for too soon CMND flag.
131	SAR Time Long	Check if CMND flag set. Check counter.
132	Write a File Mark	Check for EOR and EOF detect circuits.
141-152	Rewind Test Sub-Program	Check listing.
161	Write Ring Test Sub-Program	Check listing.
171-175	DMA Test Sub-Program	Check listing.
200-532	Extensive Read/Write Test Sub-Program	Check listing.
700	Command Flag Wait	Check listing.
701	Controller Busy	Check listing.

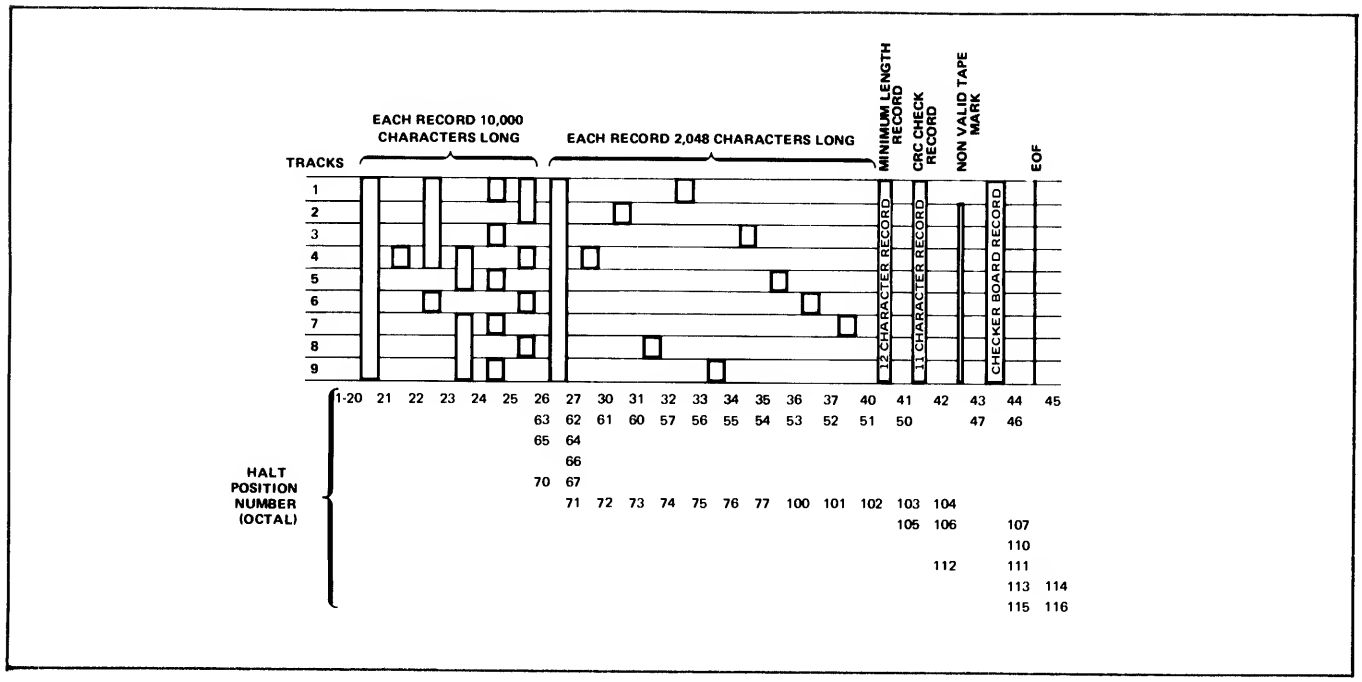


Figure 8-1. Main Diagnostic Test Pattern

8-7. ADDITIONAL TEST PROGRAMS.

8-8. Five additional tests can be added to the main program. These tests are selected by five switches of the Switch Register. Table 8-2 lists the switch settings and the options. Figure 8-2 depicts the relationship between the main diagnostic program and the tests selected by the Switch Register. Switches 13, 14, and 15 are not shown in Figure 8-2. These switches are checked by one overall error-checking subroutine which is entered after each test is made. This subroutine, called CHECK, detects errors and selects proper Teleprinter printouts. The positions of switches 13, 14, and 15 are checked by the program each time the CHECK subroutine is entered.

8-9. The five additional tests are as follows:

a. Extensive Read/Write.
b. Direct Memory Access (DMA)
c. Write Ring
d. Rewind and Start of Tape
e. Rewind and Unload.

8-10. EXTENSIVE READ/WRITE.

8-11. When Switch 1 of the SWITCH REGISTER is in the up position "1", the Extensive Read/Write tests are added to the diagnostic cycle, see Diagnostic Listing, page 0037. These tests consist of writing 26 records (1982 characters each) followed by 26 records (1983 characters each). The 52 records are then backspaced. The records are read, checking for data errors, length errors, and parity errors. If an error is detected while reading, the erroneous record is backspaced and reread. The data pattern for each record is as follows:

RECORD	ODD CHARACTER									EVEN CHARACTER								
(OCTAL)	P	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	P	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
1	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0
3	0	0	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0
4	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0
5	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0
6	0	0	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0
7	0	1	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0
10	0	0	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0
11	0	1	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0
12	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0
13	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1
14	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0
15	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0
16	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0
17	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0
20	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0
22	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	1	0	0
23	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	1
24	1	1	1	1	0	0	1	1	1	0	0	0	0	1	0	0	0	0
25	0	1	1	0	1	0	1	1	1	1	0	0	1	0	0	0	0	0
26	0	1	1	0	1	0	1	1	1	1	0	0	1	0	0	0	0	0
27	1	1	0	1	1	0	1	1	1	0	0	1	0	0	0	0	0	0
30	1	0	1	1	1	0	1	1	1	0	1	0	0	0	0	0	0	0
31	0	1	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0
32	1	1	1	1	1	0	0	1	1	0	0	0	0	0	1	0	0	0

Table 8-2. Switch Register Selections

SWITCHES									OPTION SELECTED
15	14	13	12	4	3	2	1	0	
								1	Rewind at end of main diagnostic program and perform Start of Tape (SOT) tests.
							1	X	Perform extensive Read-Write tests prior to operation specified by Switches 0, 2, and 3.
						1	X	X	Perform Write-Ring (Write Enabled) test after the main diagnostic program.
					1	X	X	X	Rewind and unload after operations performed by switches 0, 1, and 2.
				1	X	X	X	X	DMA test performed.
			1	X	X	X	X	X	Halt after current diagnostic cycle; print number of cycles completed.
		1	X	X	X	X	X	X	Halt after error detected; Computer halts with Halt Position No. in the B-Register and tape unit status in the A-Register.
0	1	0	—	—	—	—	—	—	Recycle through current test continually, bypassing error typeout.
1	X	X	—	—	—	—	—	—	Halt after current test; Computer halts with Halt Position No. in the B-Register and tape unit status in the A-Register.

NOTES:
0 = Switch in down (off) position.
1 = Switch in up (on) position.
X = Switch is on or off as required to form multiple options.
— = Position of switch is immaterial. It has no effect on option selected.

8-12. DIRECT MEMORY ACCESS (DMA) TEST.

8-13. When switch 4 of the SWITCH REGISTER is in the up position, the DMA test is added to the diagnostic cycle, see Diagnostic Listing, page 0037. A 700 character record is written using a DMA channel. The character record is backspaced over and read using the DMA channel.

8-14. WRITE RING TEST.

8-15. When switch 2 of the SWITCH REGISTER is in the up position, the Write Ring Test is added to the diagnostic cycle, see Diagnostic Listing, page 0039. The Teleprinter types out when to remove the plastic write ring from the tape supply reel. When the plastic write ring is removed and the Magnetic Tape Unit is in AUTO, press Computer RUN. If an error message is not printed the write enable test is completed. Replace the plastic write ring, put the Magnetic Tape Unit in AUTO mode and press Computer RUN.

8-16. REWIND AND START OF TAPE TEST (SOT).

8-17. When switch 0 of the SWITCH REGISTER is in the up position, the Rewind and SOT tests are added to the cycle, see Diagnostic Listing, page 0040. The reel of tape is rewound and a rewind command and backspace command is given at the Start of Tape.

8-18. REWIND AND UNLOAD.

8-19. When switch 3 of the SWITCH REGISTER is in the up position, the Rewind and Unload test is added to the diagnostic, see Diagnostic Listing, page 0041. The tape reel is rewound and the magnetic tape unit is switched to LOCAL and the Computer halts.

8-20. TELEPRINTER PRINTOUTS.

8-21. A Teleprinter must be connected to the Computer during use of the diagnostic program to provide printouts of detected errors. When an error occurs, the Teleprinter

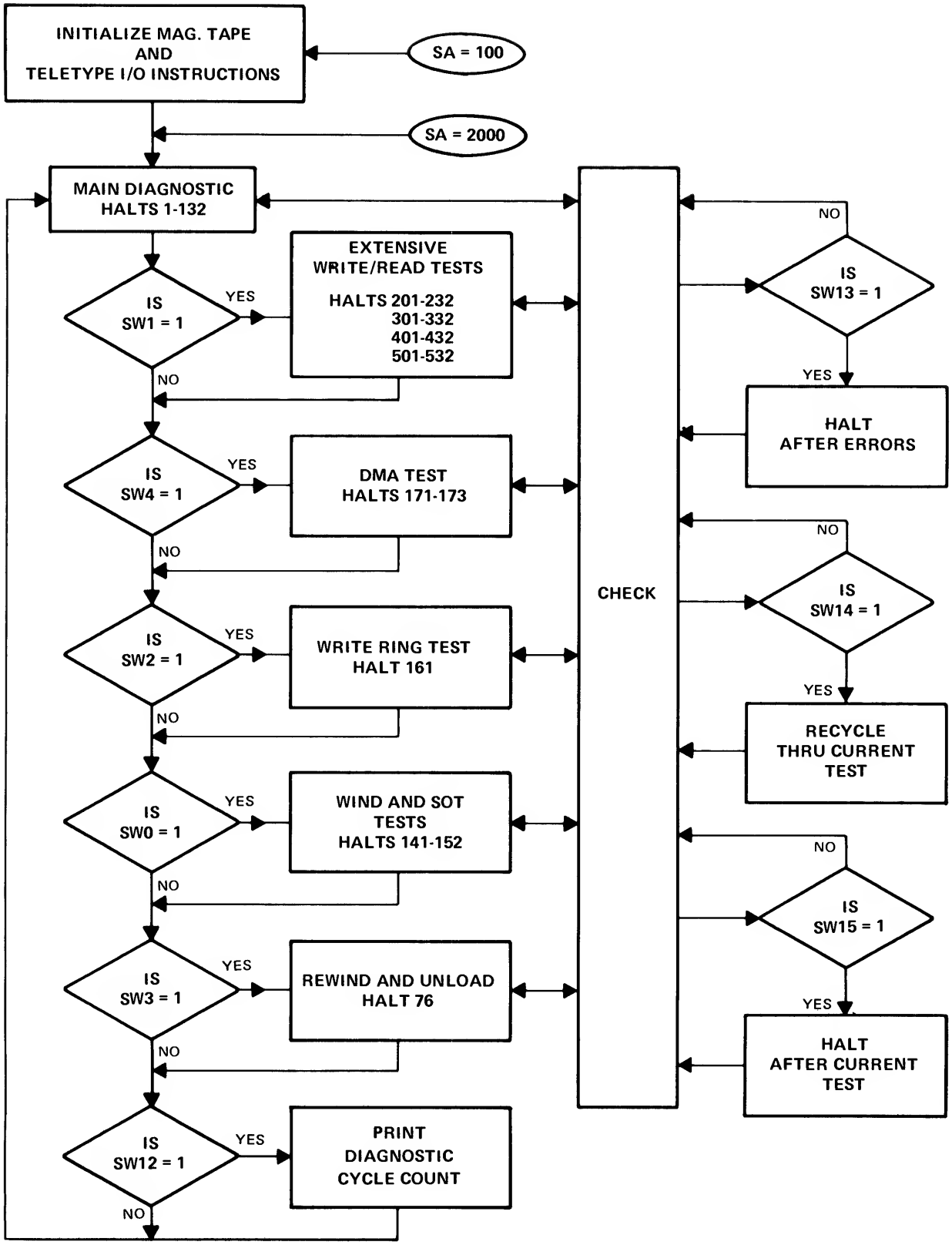


Figure 8-2. Main Diagnostic and Switch Register Flow Chart

prints the number of the diagnostic cycle, the Halt Position Number preceded by "H=", and the status of the tape unit. (Performance of the main diagnostic program, with or without the five switch-selectable tests, constitutes a diagnostic cycle. The Halt Position Number identifies the specific operation being performed when the error occurred. These numbers, their operation, and trouble-shooting information is provided later in this test.) The Teleprinter printouts are as follows:

(5-digit diagnostic cycle no.)	(3-digit Halt Position No.)	(Status)
00062	H = 026	*RJ, BY

*The following status abbreviations may appear:

BY	(Busy)
PT	(Parity Error)
WS	(Write Ring missing; Write not enabled)
RJ	(Reject)
TM	(Timing Error)
ET	(End of Tape)
ST	(Start of Tape)
FM	(End of File Mark)
LS	(Local)

8-22. If a data error occurs during a read test, the Teleprinter prints the number of the first character in the record to show a data error (preceded by "C="), the character which should have been read (preceded by "G="), and the data character which was read (preceded by "B="). Also if the record is of erroneous length, the Teleprinter prints the number of extra or missing characters in the record (preceded by "L=").

EXAMPLE:

00071	H = 430		
Cycle	Halt Position		
C = 00005	G = 01110111	B = 11110111	L = 00001
Data Error	Data Character which should have been read	Data Character Read	Extra Characters

8-23. Therefore, on diagnostic cycle 71, a data error was flagged on the extensive read/write test. The fifth character in the record picked up a bit in the most significant position. The record was also one character too long.

8-24. SECONDARY PROGRAMS.

8-25. Four Secondary Programs which provide more detailed troubleshooting analysis are as follows:

a. Write/read reflection test.
b. Magnetic tape command repertoire test.
c. Data pattern test.
d. D-3030 Set-up an exercise test.

8-26. WRITE/READ REFLECTION TEST.

8-27. This program is entered into memory location 1000 (see Diagnostic Listing, page 0018). The program writes the Switch Register bits 0-7 onto tape and reads the information back into the B-Register. With switch 15 of the SWITCH REGISTER in the up position, 1, the Computer halts.

8-28. MAGNETIC TAPE COMMAND REPERTOIRE TEST.

8-29. This program is entered into memory location 1100 (see Diagnostic Listing, page 0019). The program outputs the Switch Register every 1 millisecond, 5 milliseconds or 150 milliseconds depending on the position of switches 14 and 15 of the SWITCH REGISTER.

PERIOD	SWITCH 14	SWITCH 15
1 ms	0	0
5 ms	1	0
150 ms	1	1

8-30. DATA PATTERN TEST.

8-31. This program is entered into memory location 1200, see Diagnostic Listing, page 0019. This program writes the bits located in the Switch Register. Bit 0 through 7 are written on tape, then bits 8 through 15 are written on tape. This alternating procedure continues. With switch 15 of the SWITCH REGISTER in the up position, the Computer halts.

8-32. D-3030 SET-UP AND EXERCISE TEST.

8-33. This program is entered into memory location 1300 (see Diagnostic Listing, page 0020). The program can be used to set-up the Magnetic Tape Unit. Switches 0 through 9 are used to test the various operations. Only one switch at a time can be in the up position. To stop the operation, put the switch down. The end of tape is automatically checked. The various operations and switches are as follows:

SWITCH 0	Write
SWITCH 1	Write a file mark record
SWITCH 2	Gap
SWITCH 3	Read
SWITCH 4	Forward space
SWITCH 5	Backspace
SWITCH 6	Rewind
SWITCH 7	Unload
SWITCH 8	Start stop forward
SWITCH 9	Start stop backward

8-34. CONDENSED OPERATING PROCEDURES.

8-35. The following is a condensed operating procedure for this diagnostic.

a. Load diagnostic tape using the ABL.

b. S.A. = 100B.

c. Sw Reg = select code of data channel. Set bit 15 if HP 2115 or 2114 computer.

d. RUN

e. HLT Ø. P Reg = 000121.

f. Sw. Reg = Select code of TTY. Set bit 15 for serial.

g. RUN

h. HLT Ø. P Reg = 000127.

i. Sw. Reg = last memory address.

j. RUN

k. HLT Ø. P Reg = 000134.

l. Thread and load a scratch tape with Write Ring on tape unit. Set to 800 bpi and switch to AUTO.

m. Switch Options:
1) Bit Ø = 1 Rewind and BOT Test
2) Bit 1 = 1 Extensive Read/Write Test
3) Bit 2 = 1 Write Ring Test
4) Bit 3 = 1 Rewind & Unload Test (refer to step "r")
5) Bit 4 = 1 DMA Test

n. Set Sw. Reg options and RUN.

o. If no options selected, program will loop through the basic test.

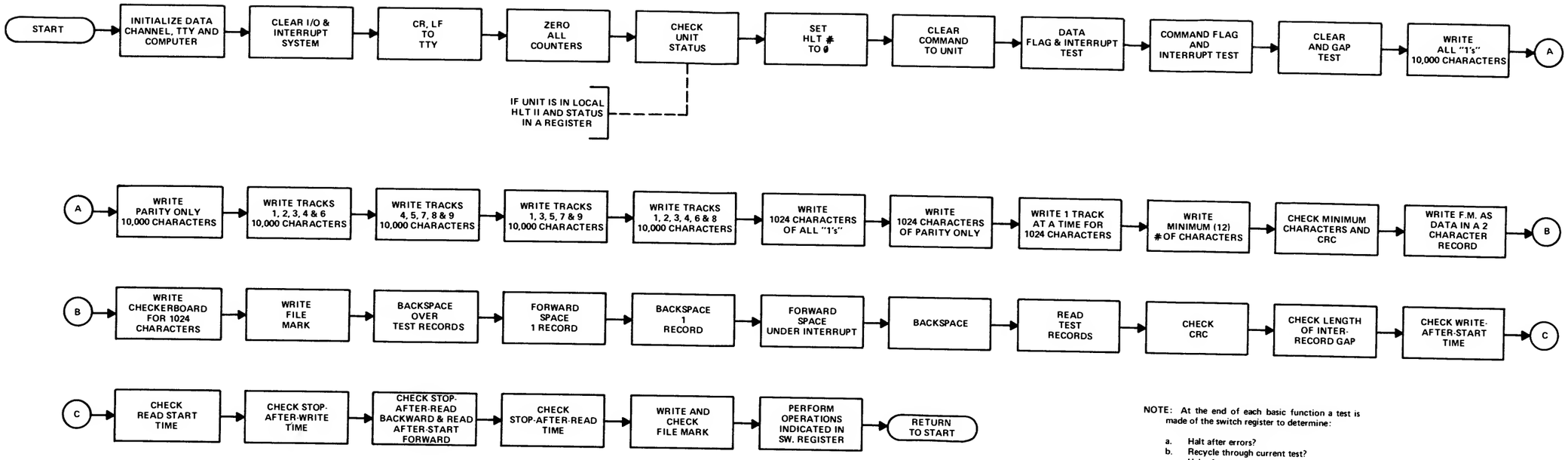
p. During execution the following switch options are available:
1) Bit 12 = 1 Print cycle count
2) Bit 13 = 1 Halt after errors
3) Bit 14 = 1 Recycle through current test
4) Bit 15 = 1 Halt after current test (restart address 2000B)

q. The following secondary programs are available:

1) S.A.=1000B Write Sw. Reg bits 0-7 and read back into B Reg. Bit 15 halts program.
2) S.A.=1100B Output command in Sw. Reg bits 0-7 every 1 ms (bits 14 + 15 = 0), 5 ms (bit 14 = 1) or 150 ms (bits 14 + 15 = 1). Depress HALT to stop program. (Refer to step "r".)
3) S.A.=1200B Write entire Sw. Reg continuously. Bit 15 halts program.
4) S.A.=1300B Set up & exercise test. Only one bit in Sw. Reg. may be set at one time. Program loops in specified test until switch cleared.

Bit Ø = Write
Bit 1 = Write File Mark
Bit 2 = Gap
Bit 3 = Read
Bit 4 = Forward Space
Bit 5 = Backspace
Bit 6 = Rewind
Bit 7 = Unload (Refer to step "r")
Bit 8 = Start-Stop Forward
Bit 9 = Start-Stop Reverse

r. If an UNLOAD operation is performed, in order to restart the tape unit must be switched to AUTO and the computer PRESET. Restart address is 2000B.



NOTE: At the end of each basic function a test is made of the switch register to determine:

a. Halt after errors?
b. Recycle through current test?
c. Halt after current test?

At the end of the Main Program a test is made of the switch register to determine:

a. Perform extensive read/write test?
b. Perform DMA test?
c. Perform Write ring test?
d. Perform rewind and start-of-tape test?
e. Perform rewind and unload test?
f. Print cycle count?

Figure 8-3. Diagnostic, Main Program

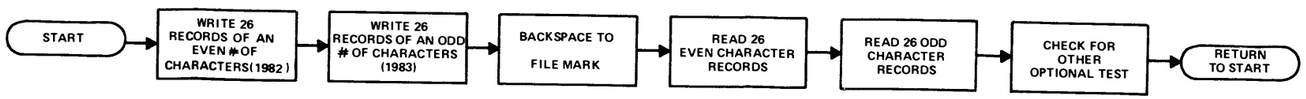


Figure 8-4. Sub-Program, Extensive Read/Write

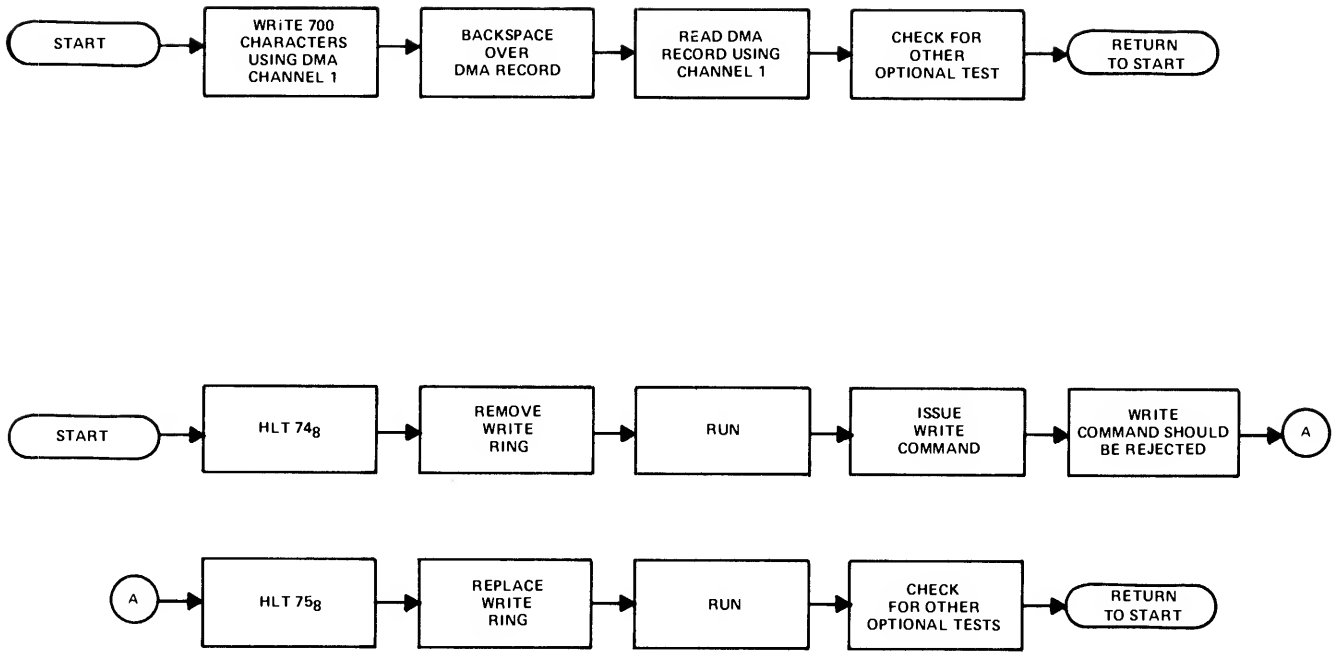


Figure 8-5. Diagnostic Sub-Program, DMA & Write Ring Test

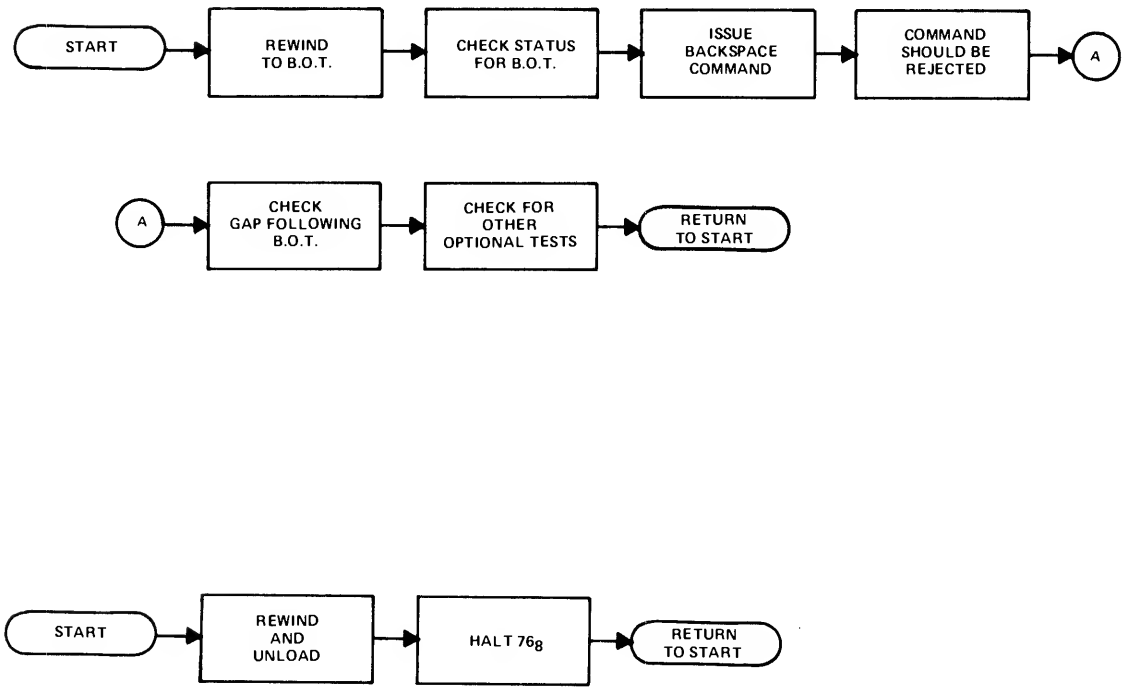


Figure 8-6. Diagnostic Sub-Program, Rewind & Rewind Unload Tests

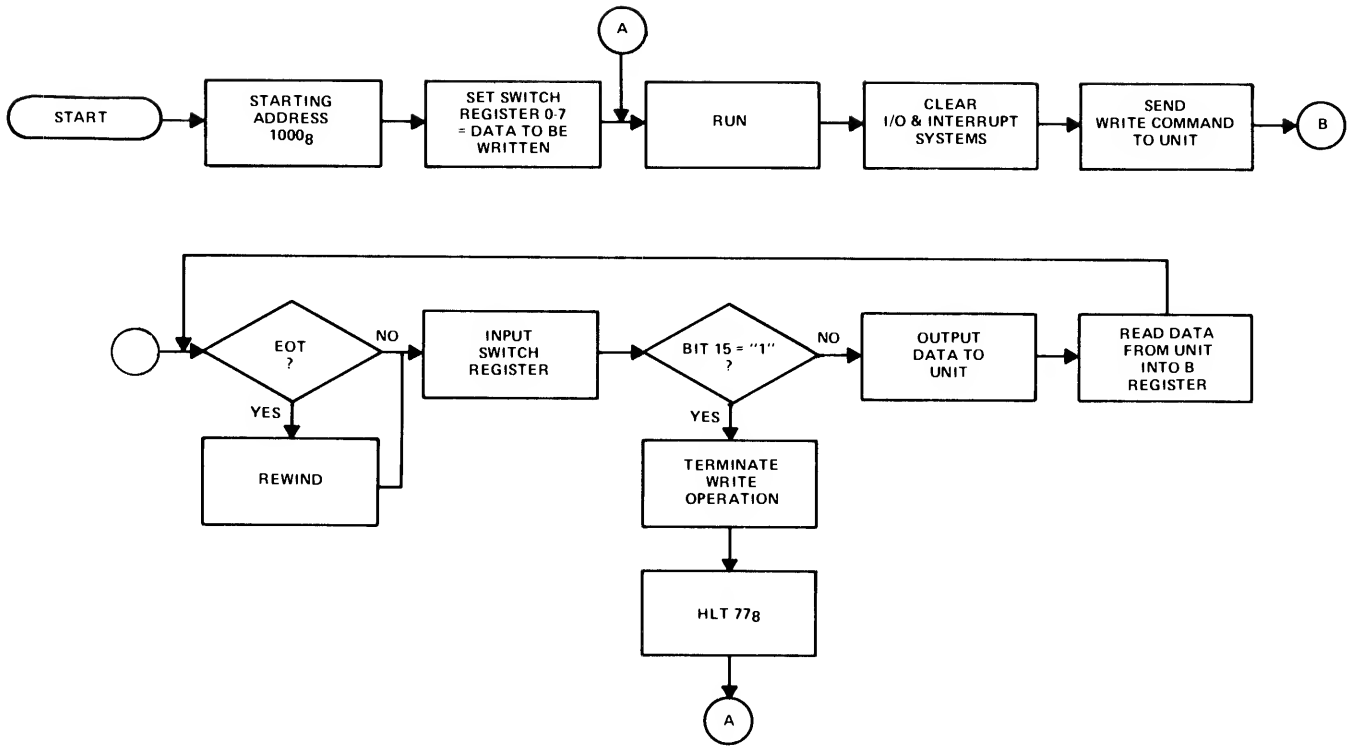


Figure 8-7. Diagnostic Subsidiary Debugging Program,
Write Switch Register Bits 0 - 7
Read Into B Register

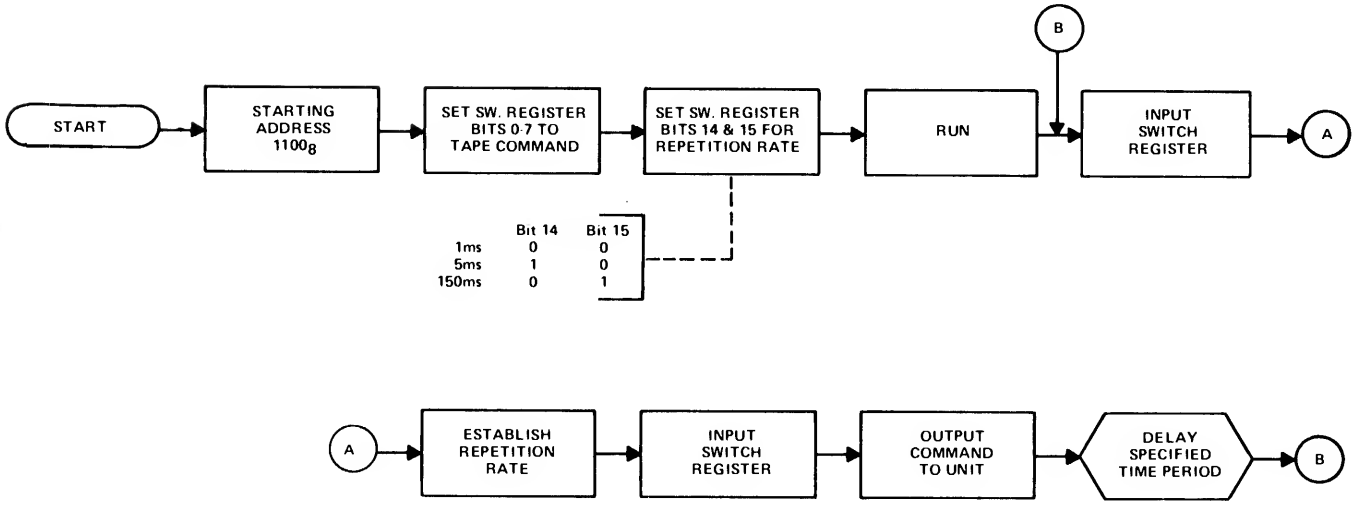
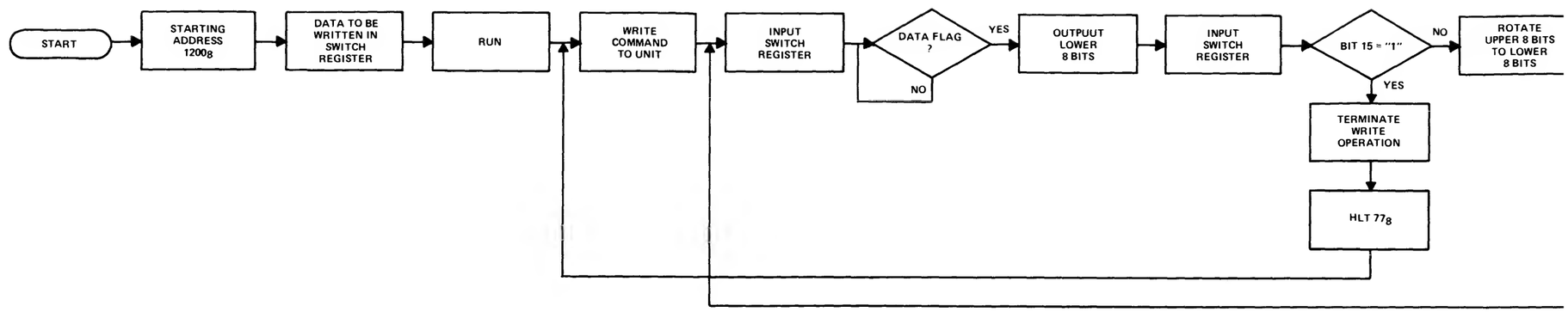
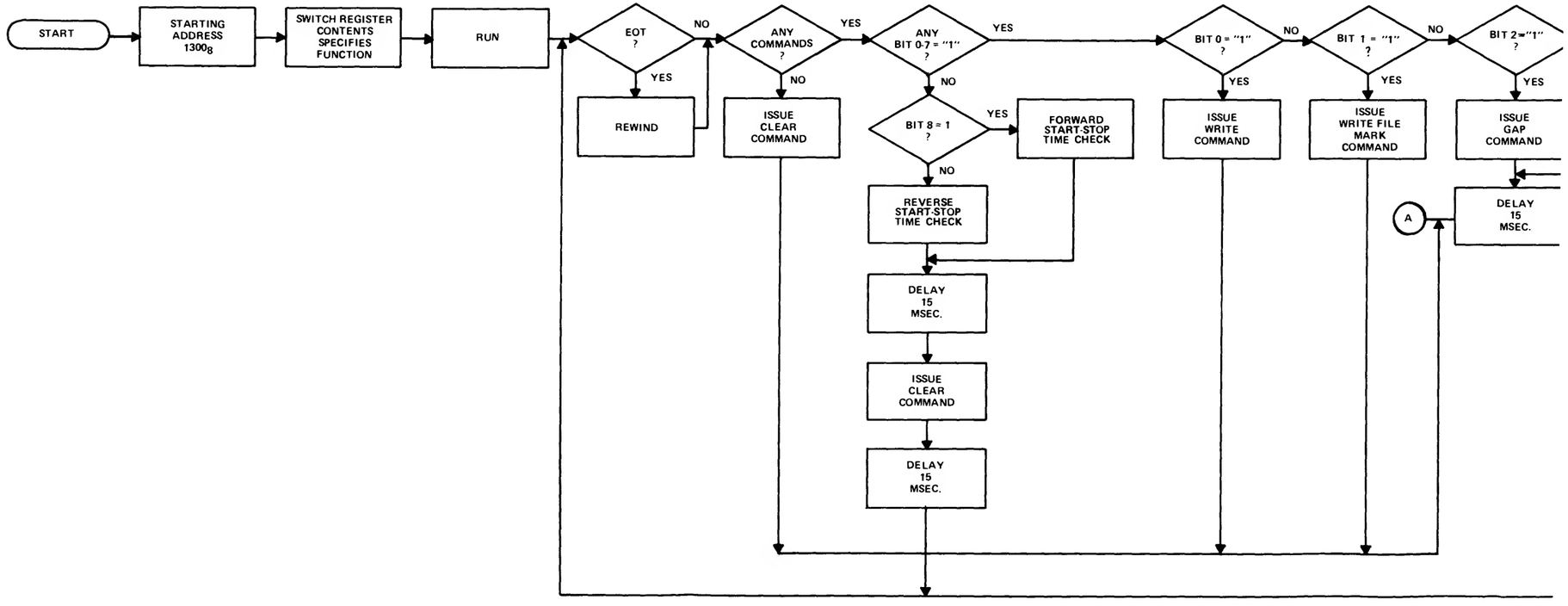


Figure 8-8. Diagnostic, Subsidiary Debugging Program,
Command Test


START
STARTING ADDRESS 1200$_8$
DATA TO BE WRITTEN IN SWITCH REGISTER
RUN
WRITE COMMAND TO UNIT
INPUT SWITCH REGISTER
DATA FLAG ?
YES
NO
OUTPUUT LOWER 8 BITS
INPUT SWITCH REGISTER
BIT 15 = "1"
NO
YES
ROTATE UPPER 8 BITS TO LOWER 8 BITS
TERMINATE WRITE OPERATION
HLT 77$_8$


START
STARTING ADDRESS 1300$_8$
SWITCH REGISTER CONTENTS SPECIFIES FUNCTION
RUN
EOT ?
NO
YES
REWIND
ANY COMMANDS ?
YES
NO
ISSUE CLEAR COMMAND
ANY BIT 0-7 = "1" ?
YES
NO
BIT 8 = 1 ?
YES
NO
FORWARD START-STOP TIME CHECK
REVERSE START-STOP TIME CHECK
DELAY 15 MSEC.
ISSUE CLEAR COMMAND
DELAY 15 MSEC.
BIT 0 = "1" ?
YES
ISSUE WRITE COMMAND
BIT 1 = "1" ?
NO
YES
ISSUE WRITE FILE MARK COMMAND
BIT 2 = "1" ?
NO
YES
ISSUE GAP COMMAND
DELAY 15 MSEC.
A

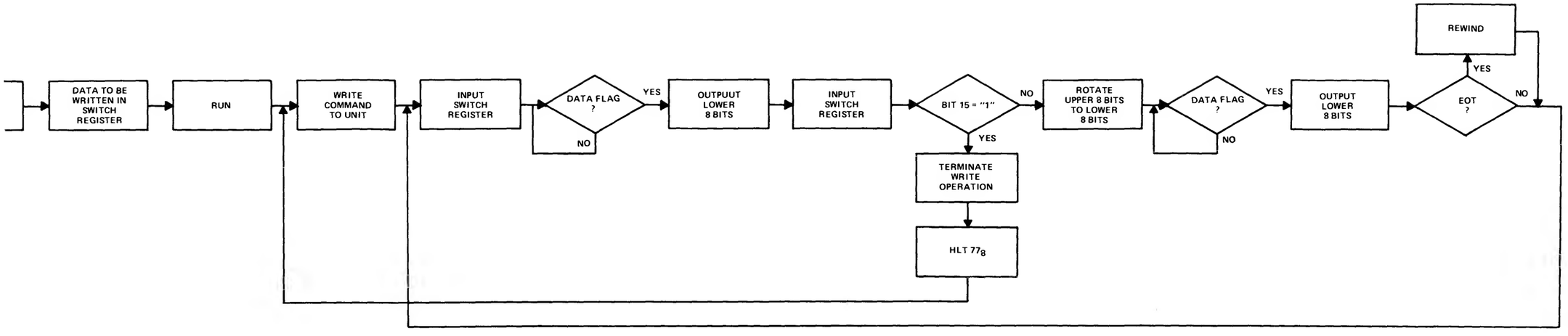


Figure 8-9. Diagnostic, Subsidiary Debugging Program, Write Switch Register Contents on Tape

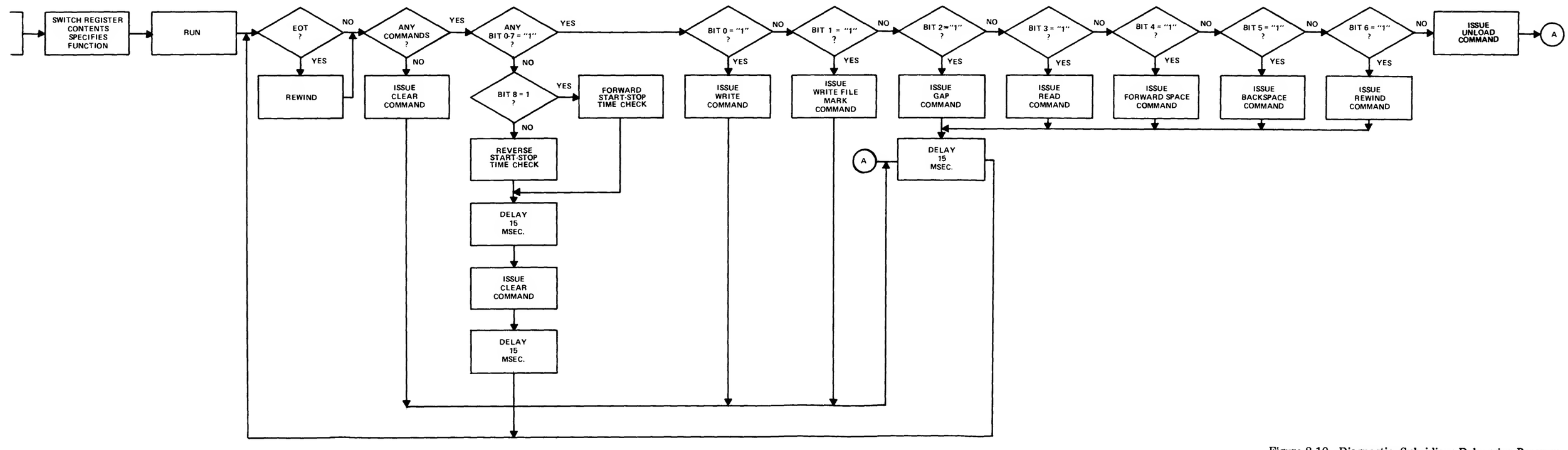


Figure 8-10. Diagnostic, Subsidiary Debugging Program, Unit Alignment